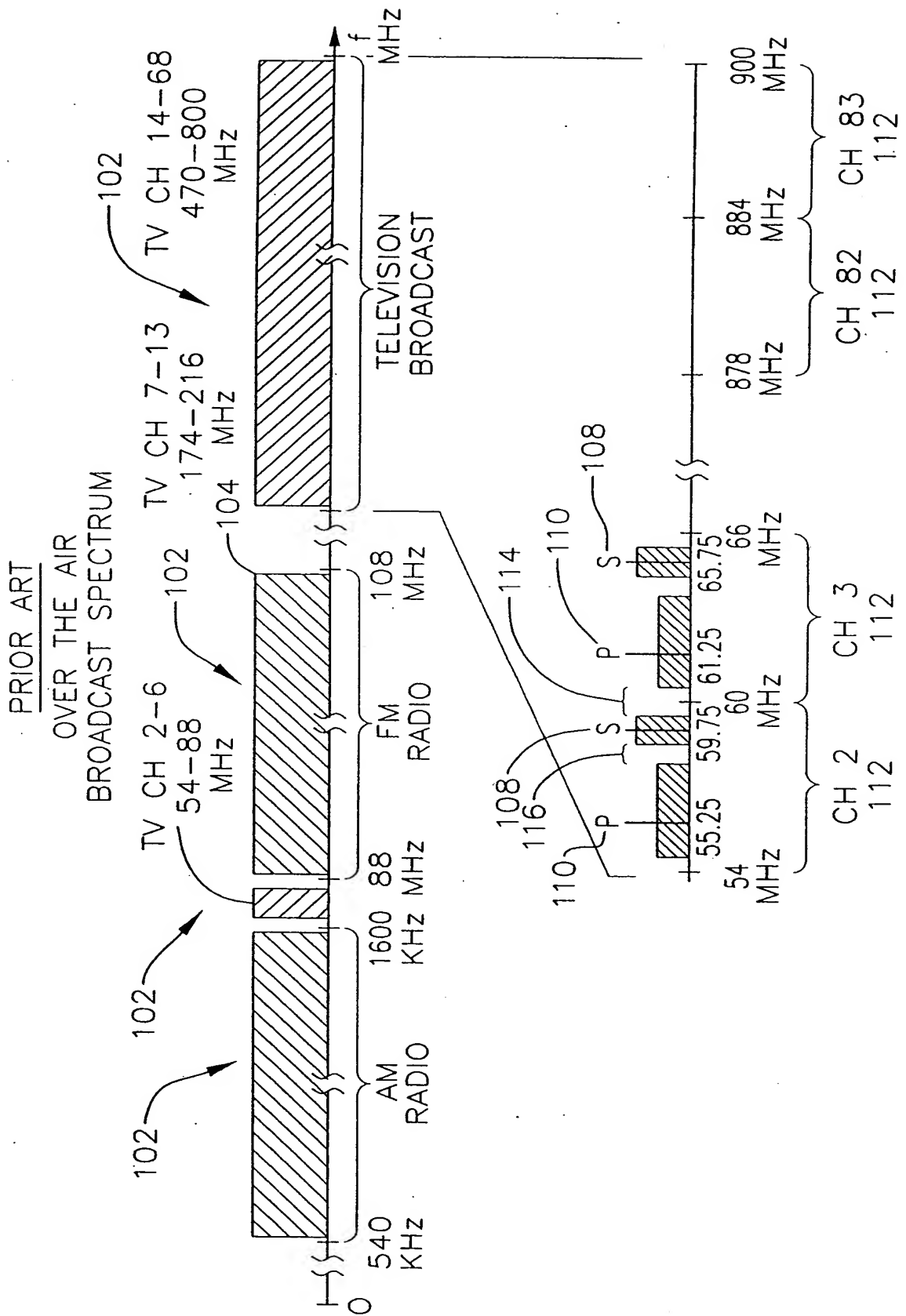
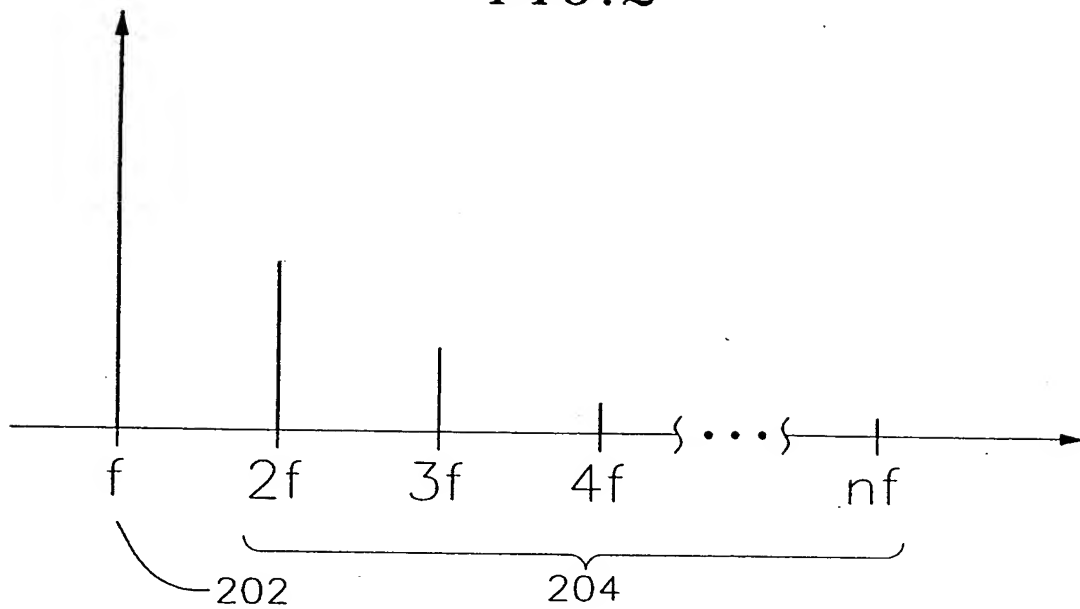


FIG. 1



**FIG. 2**



**FIG. 3**  
PRIOR ART

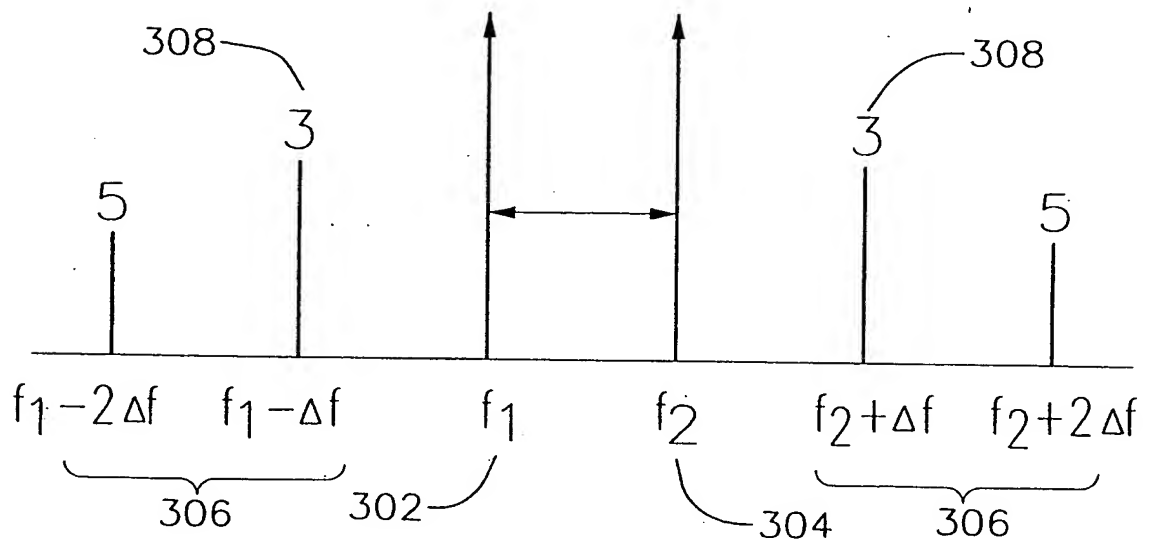
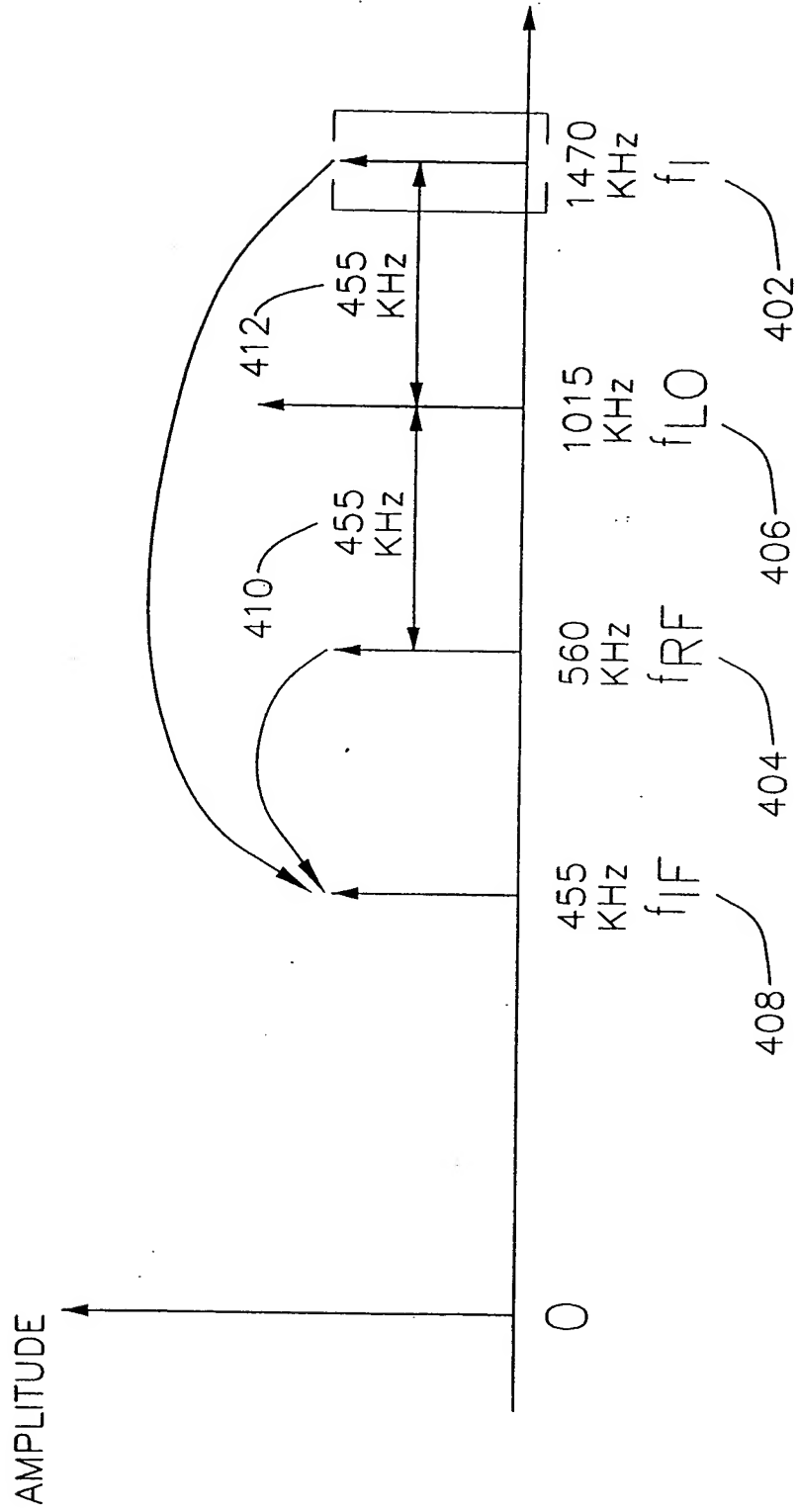
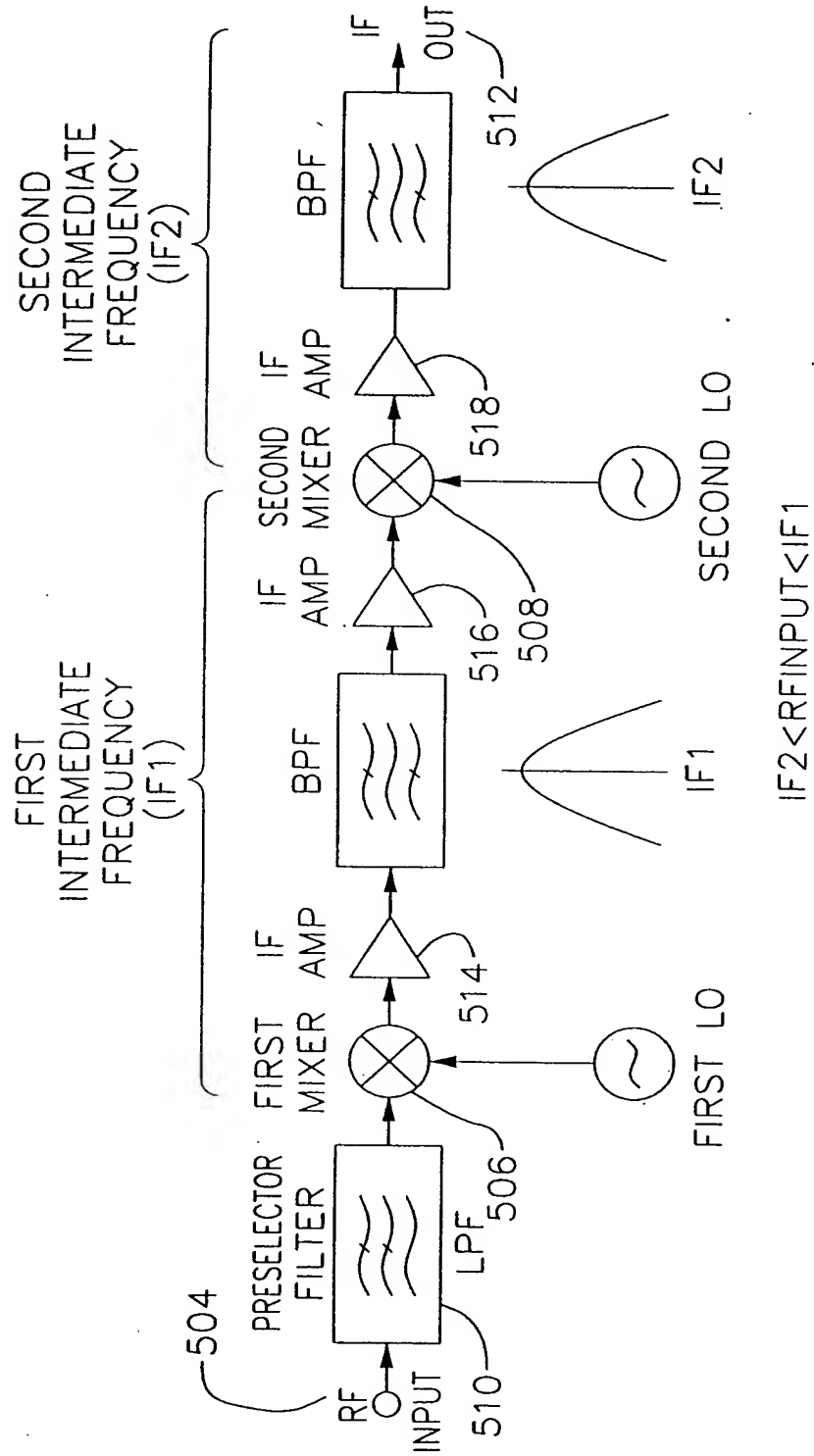


FIG. 4

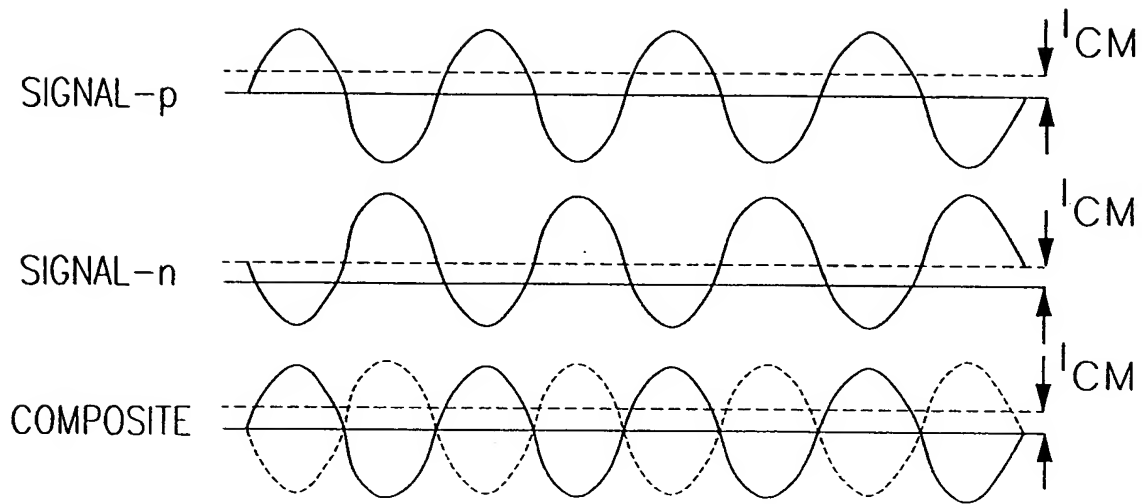
PRIOR ART



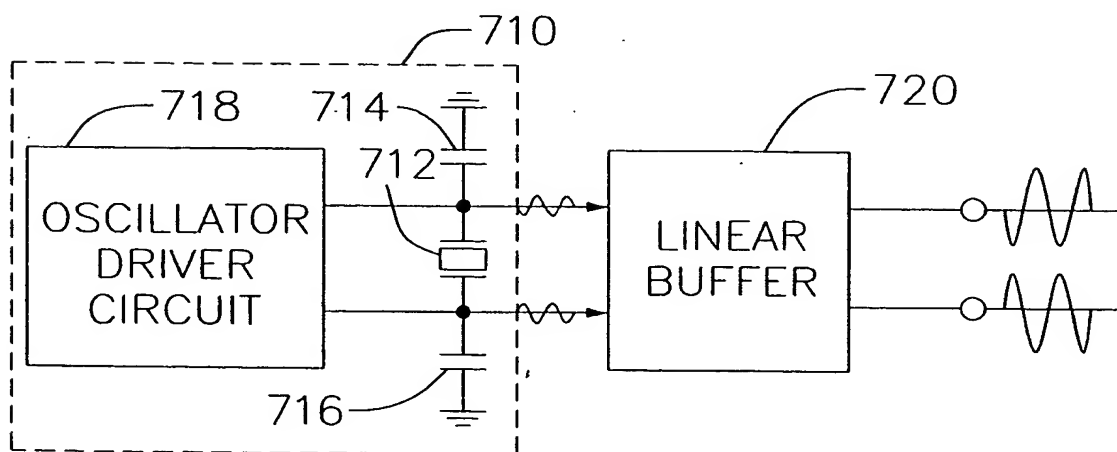
**FIG.5**  
DUAL CONVERSION RECEIVER



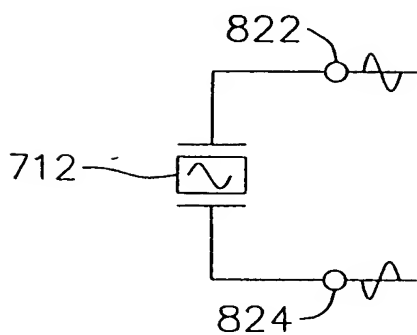
**FIG. 6**



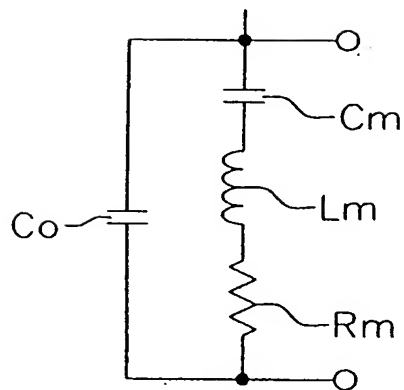
**FIG. 7**



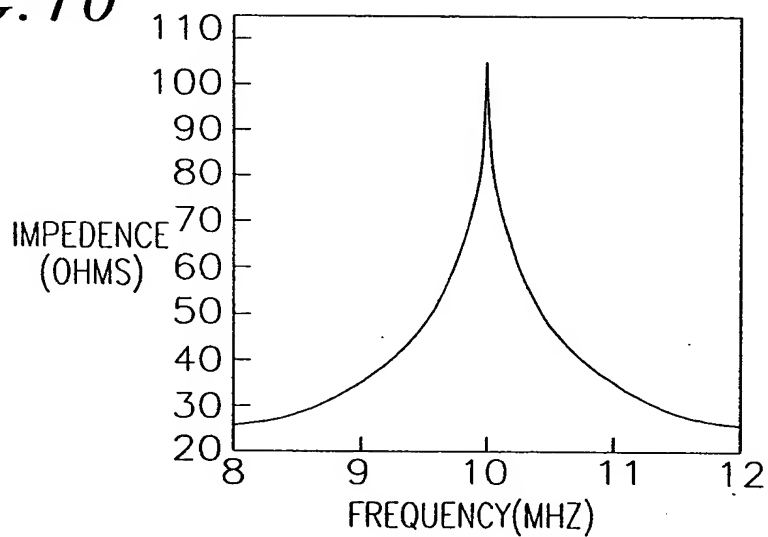
**FIG. 8**



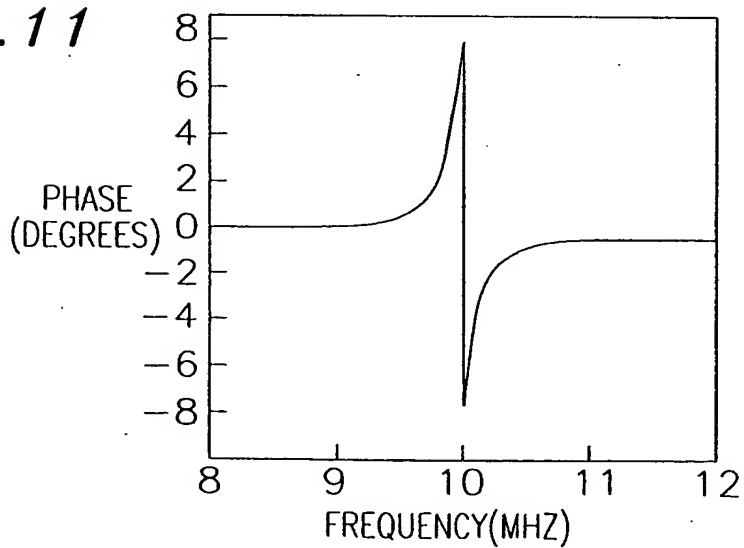
**FIG. 9**



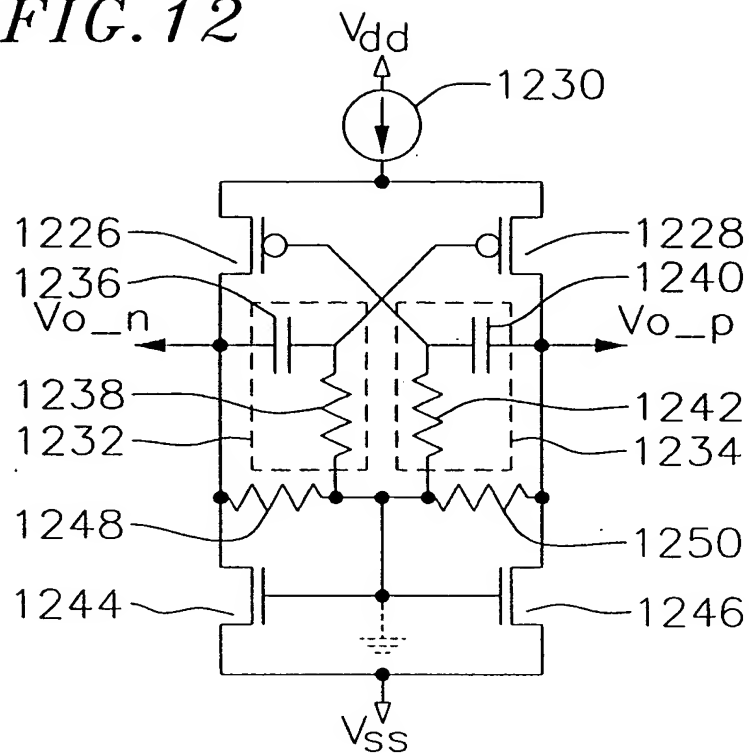
**FIG. 10**



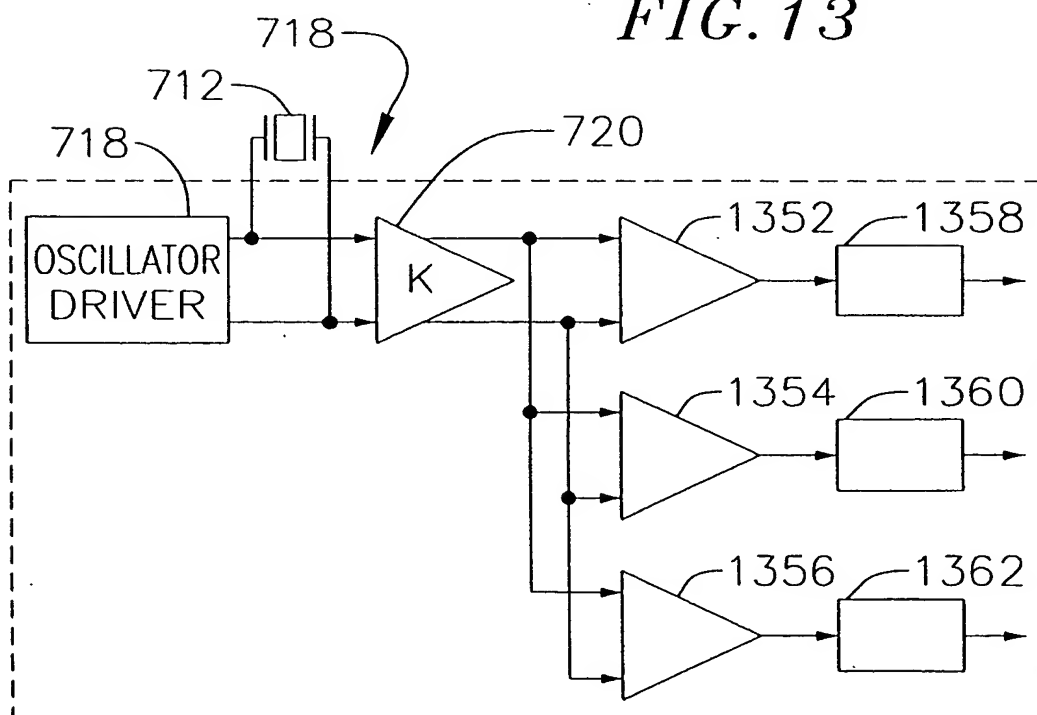
**FIG. 11**



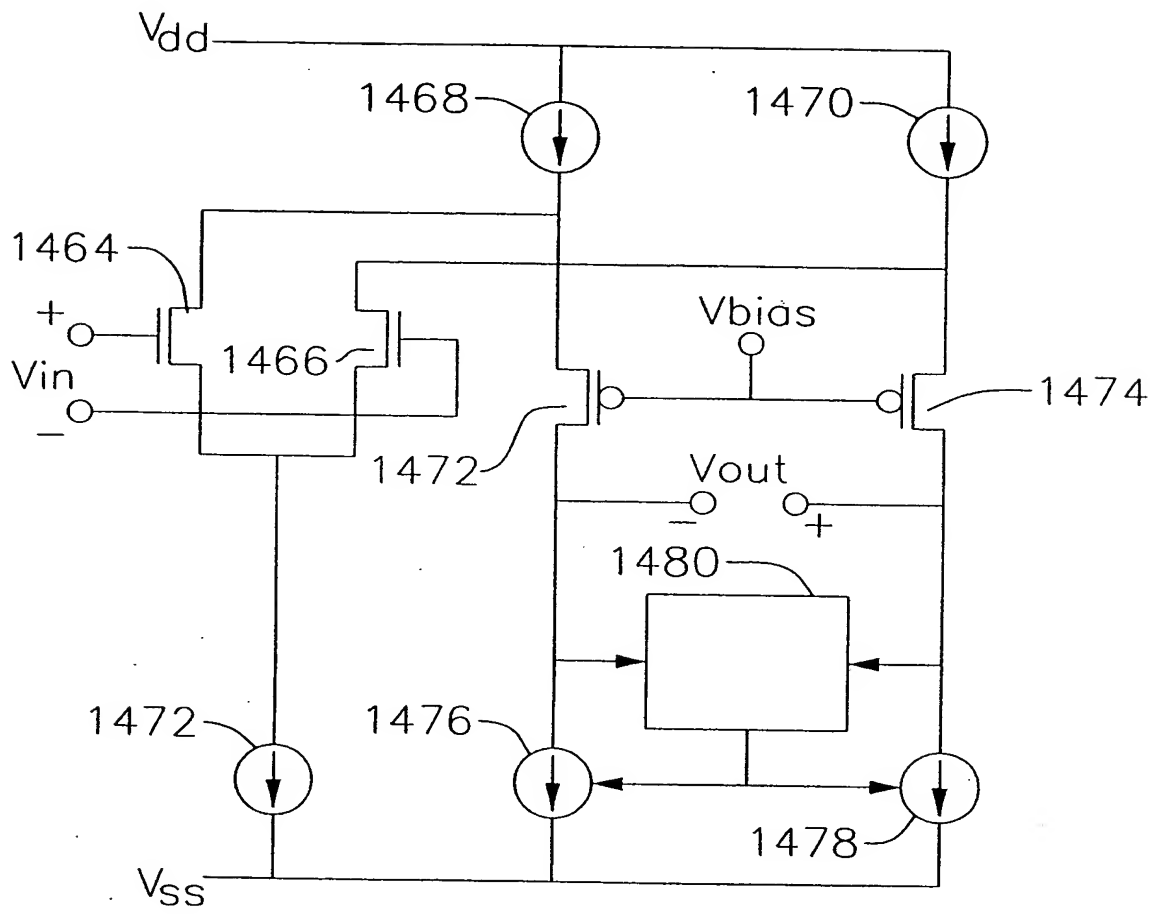
**FIG. 12**

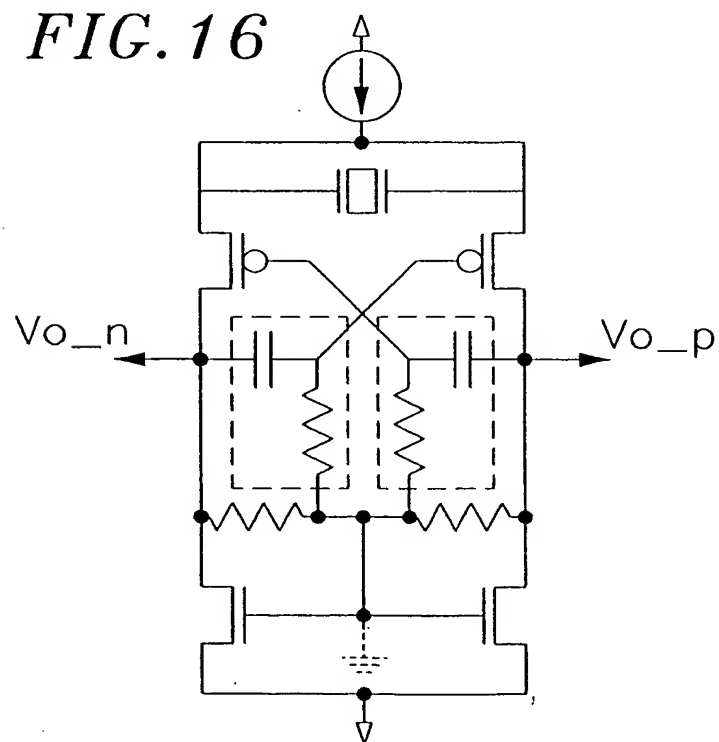
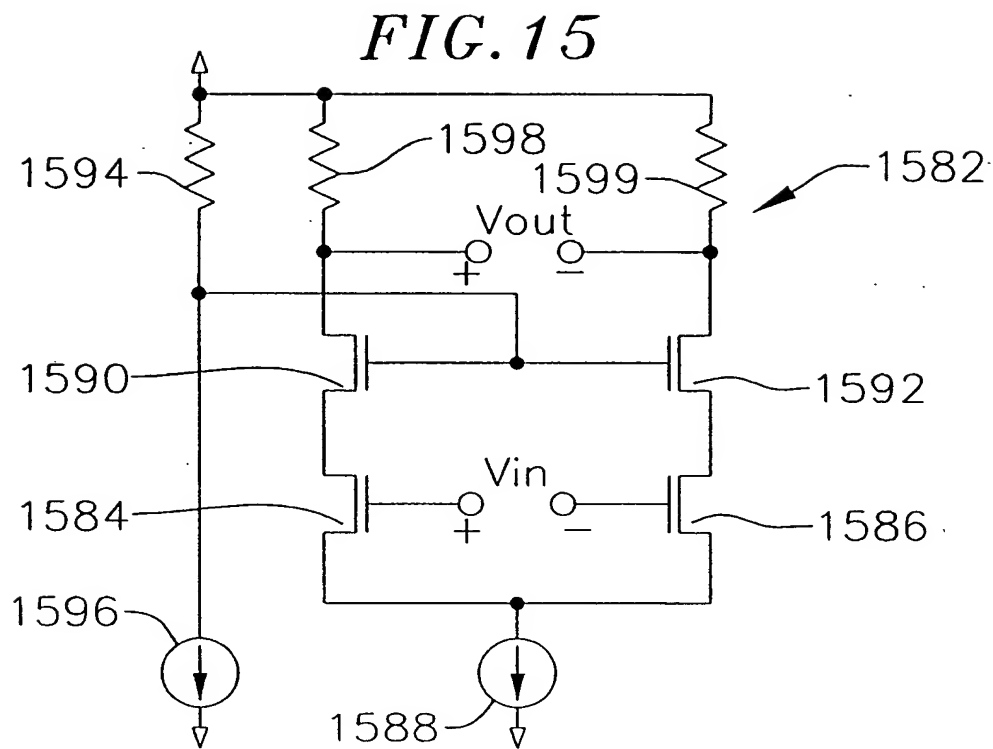


**FIG. 13**

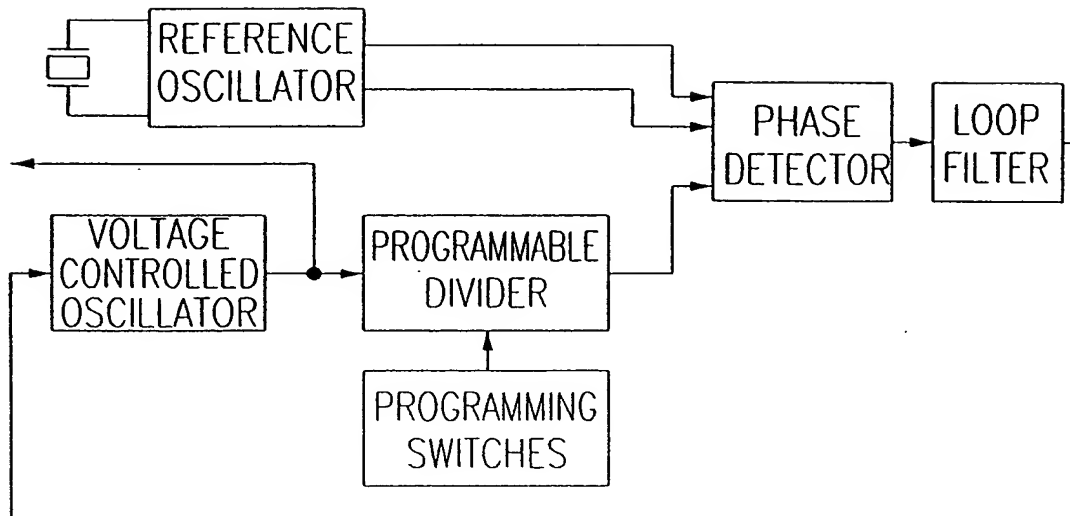


*FIG. 14*





*FIG. 17*



*FIG. 18*

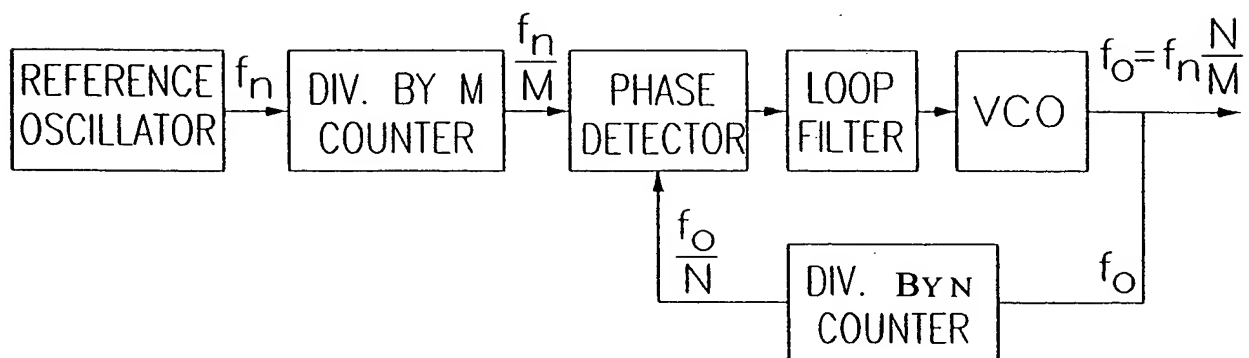


FIG. 19

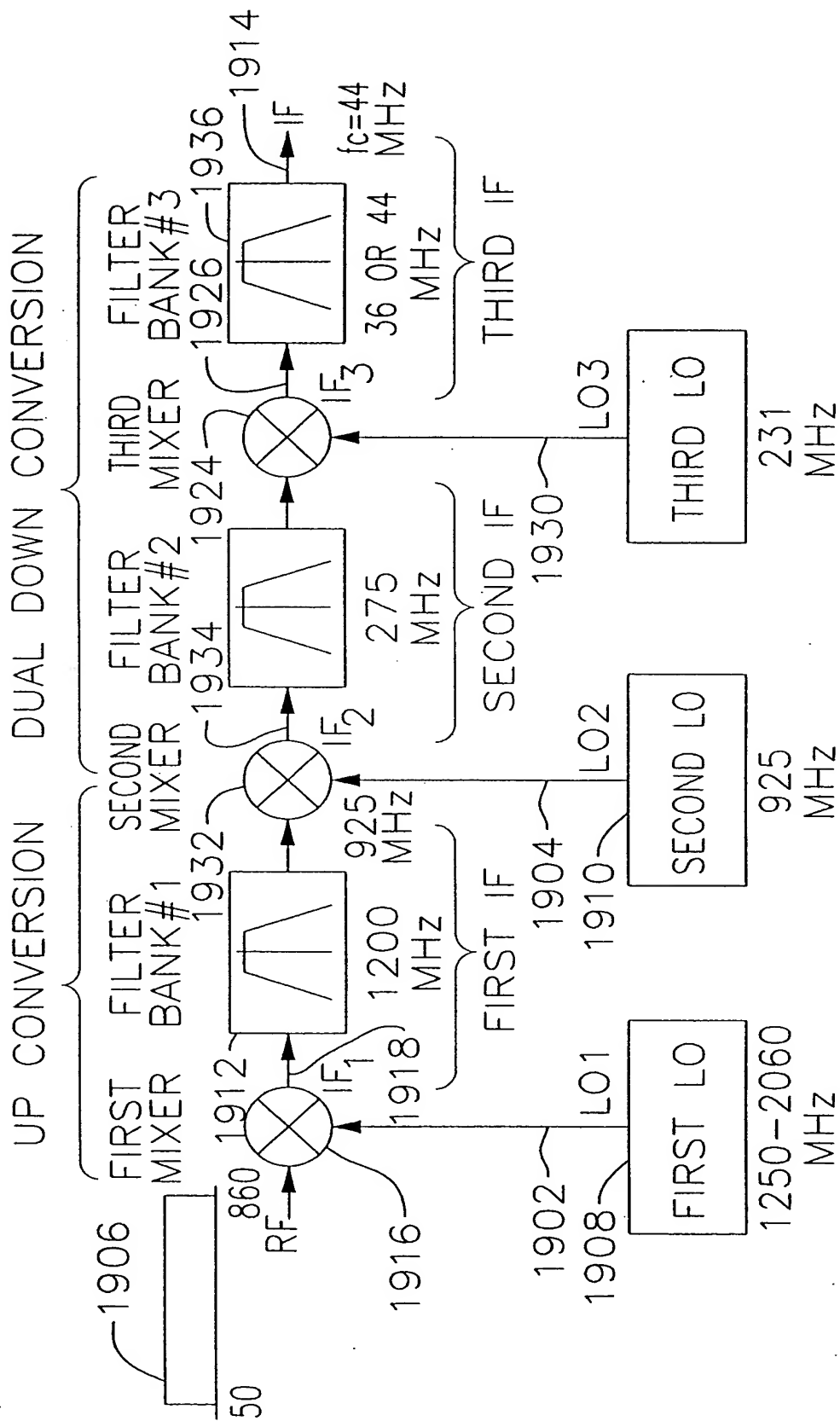
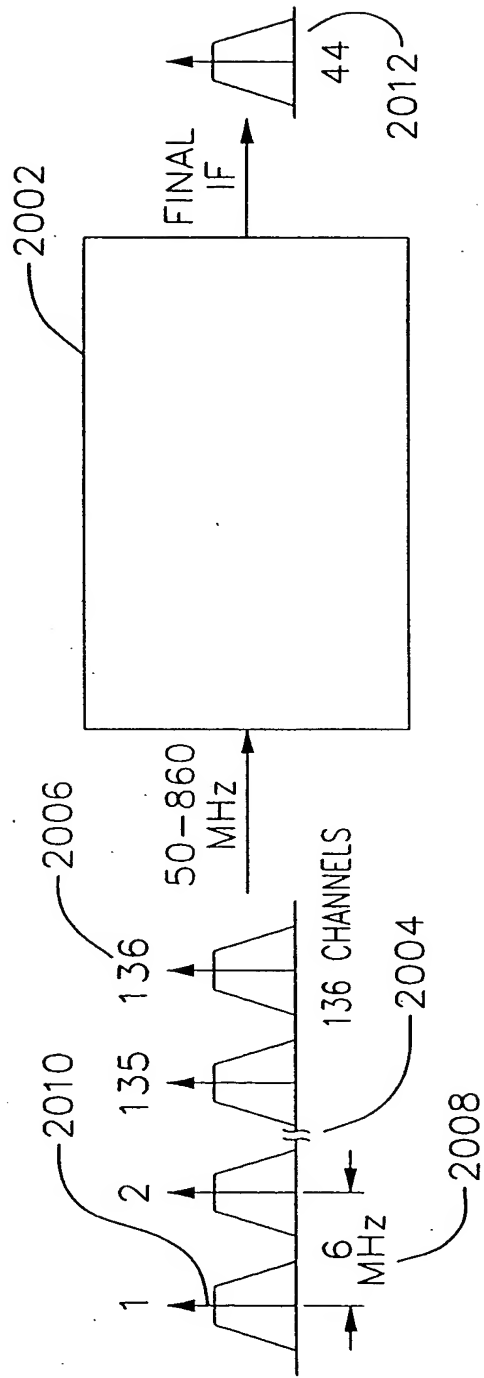


FIG. 20



PPL Xtal REFERENCE=10MHz  
 LO-1, 10MHz FREQUENCY STEPS  
 LO-2, 100kHz FREQUENCY STEPS

# FIG.21

44MHz IF

## NOTE

- LO-2 REF=100KHz  
 SO DIVIDE RANGE=9216 TO 9280

TABLE OF FREQUENCIES BASED ON  
 COARSE/FINE PLL SOLUTION:

Frf (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1 (MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	1200	1204	1198	1202	1196	1200	1204	1198	1202	1196	1200	1204	1198	1202	"	1196	1200
LO-2 (MHz)	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	"	921.6	924.8
IF-2 (MHz)	275.2	276	274.8	275.6	274.4	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	"	274.4	275.2
LO-3 (MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3 (MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

PPL Xtal REFERENCE=10MHz  
 LO-1, 10MHz FREQUENCY STEPS  
 LO-2, 100kHz FREQUENCY STEPS

FIG.22

36MHz IF

NOTE

- LO-2 REF=100KHz  
 SO DIVIDE RANGE=9280 TO 9340

TABLE OF FREQUENCIES BASED ON  
 COARSE/FINE PLL SOLUTION:

Frq (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1 (MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	1200	1202	1204	1196	1198	1200	1202	1204	1196	1198	1200	1202	1204	1196	"	1198	1200
LO-2 (MHz)	931.2	932.8	934.4	928.0	930	931	933	934	928.0	930	931	933	934	928.0	"	929.60	931.2
IF-2 (MHz)	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	"	268.4	268.8
LO-3 (MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3 (MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0

*FIG.23*

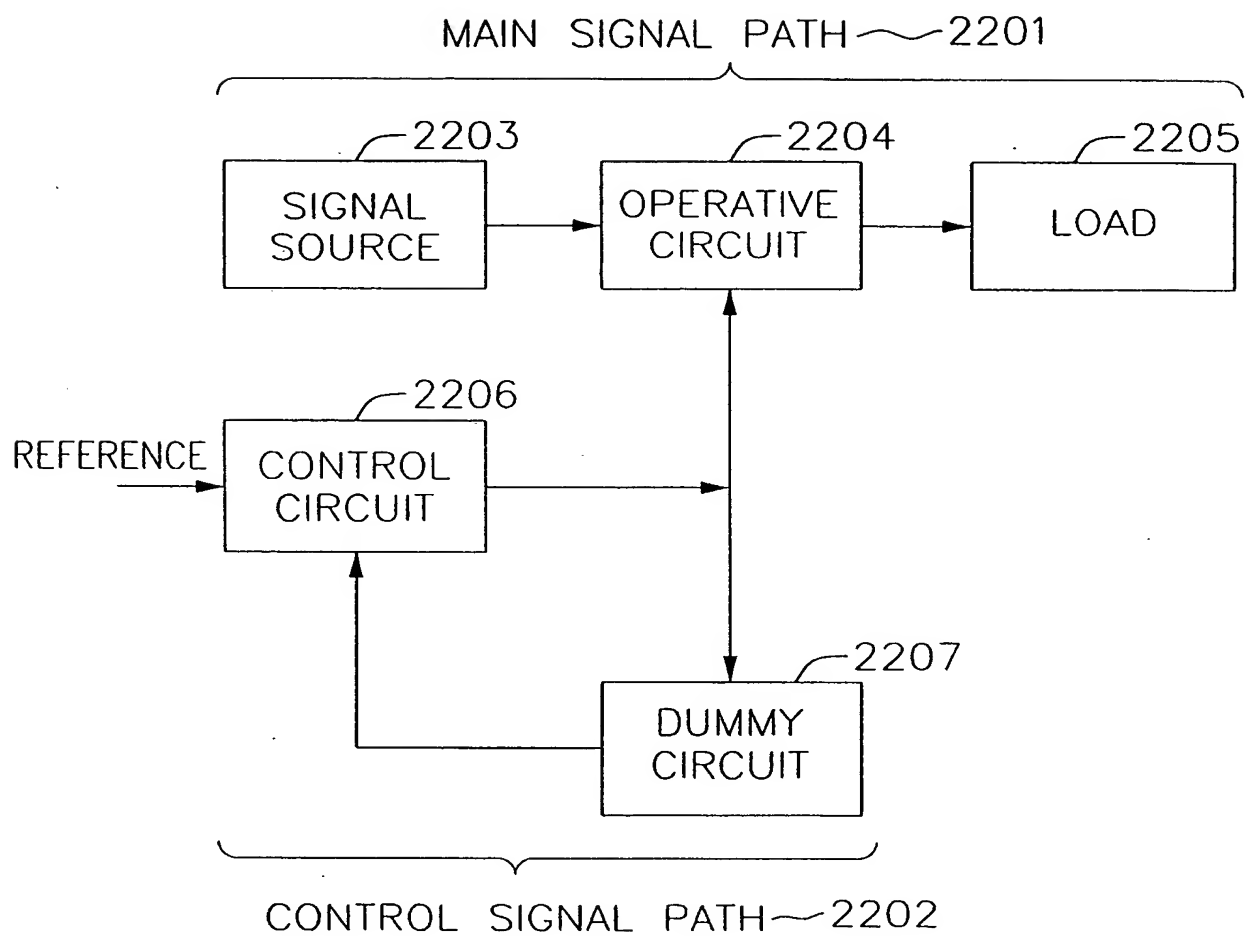


FIG. 24a

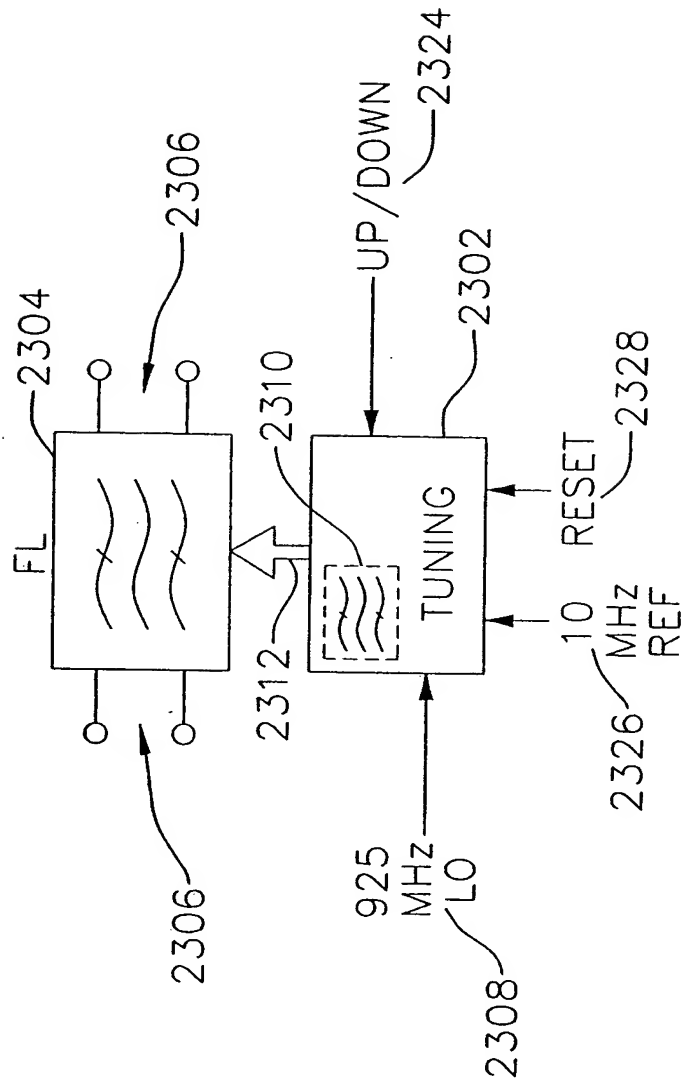


FIG. 24b

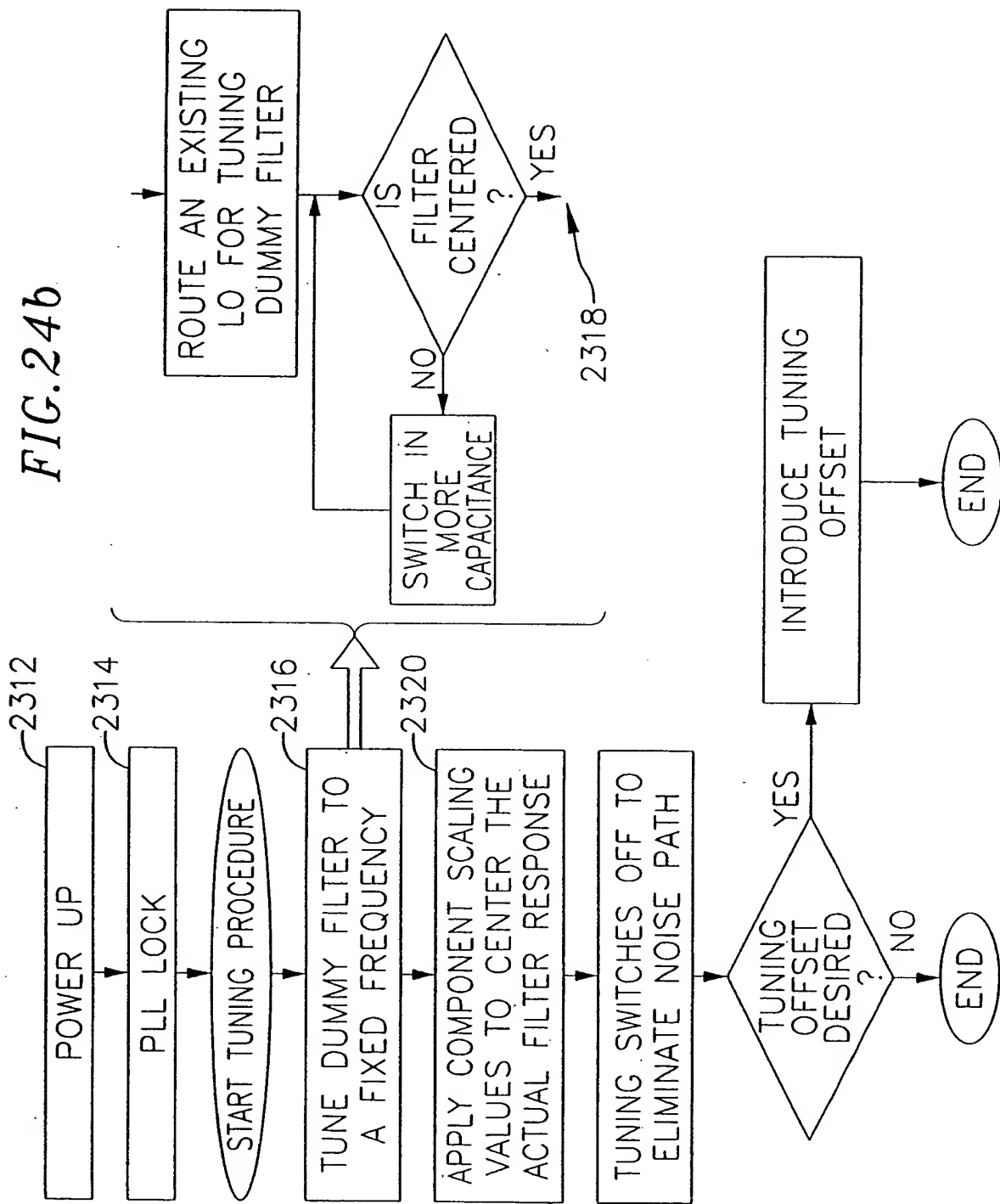


FIG. 24c

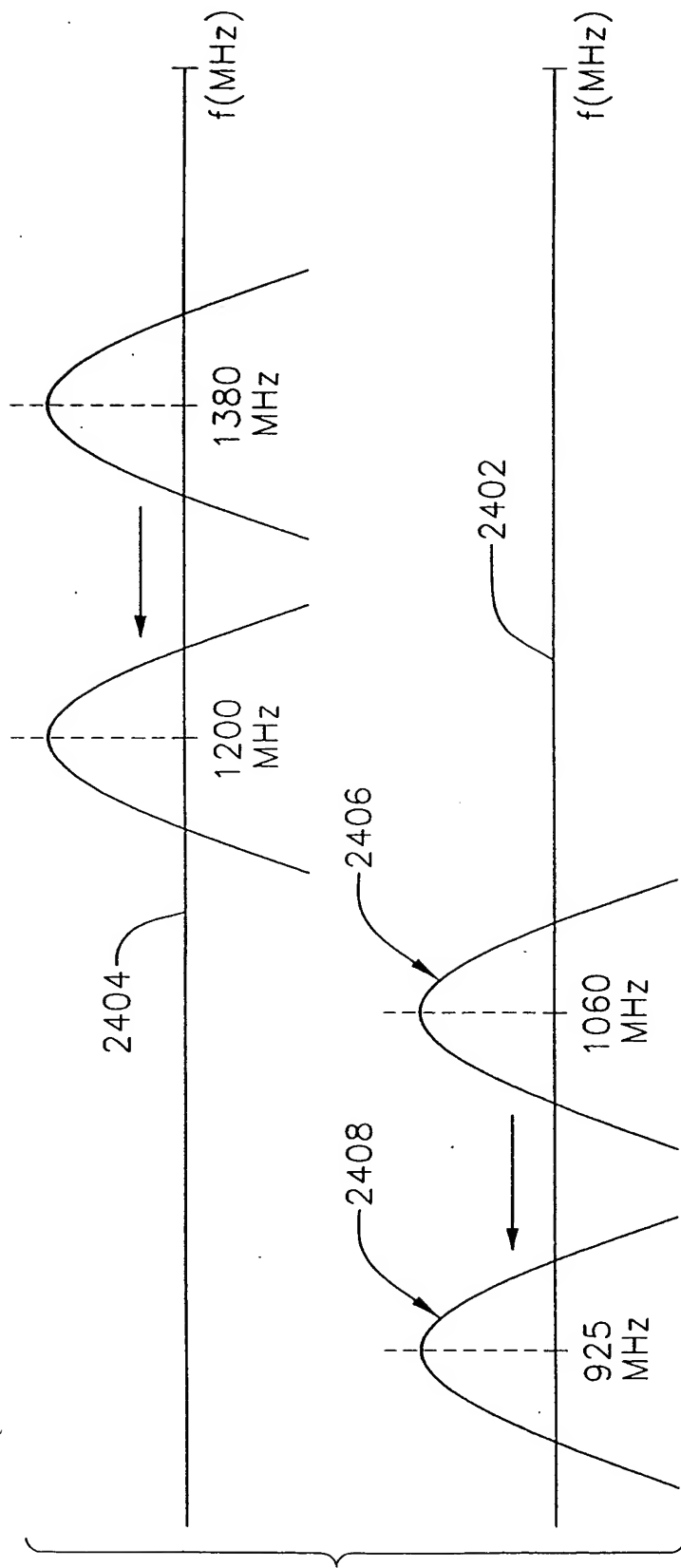
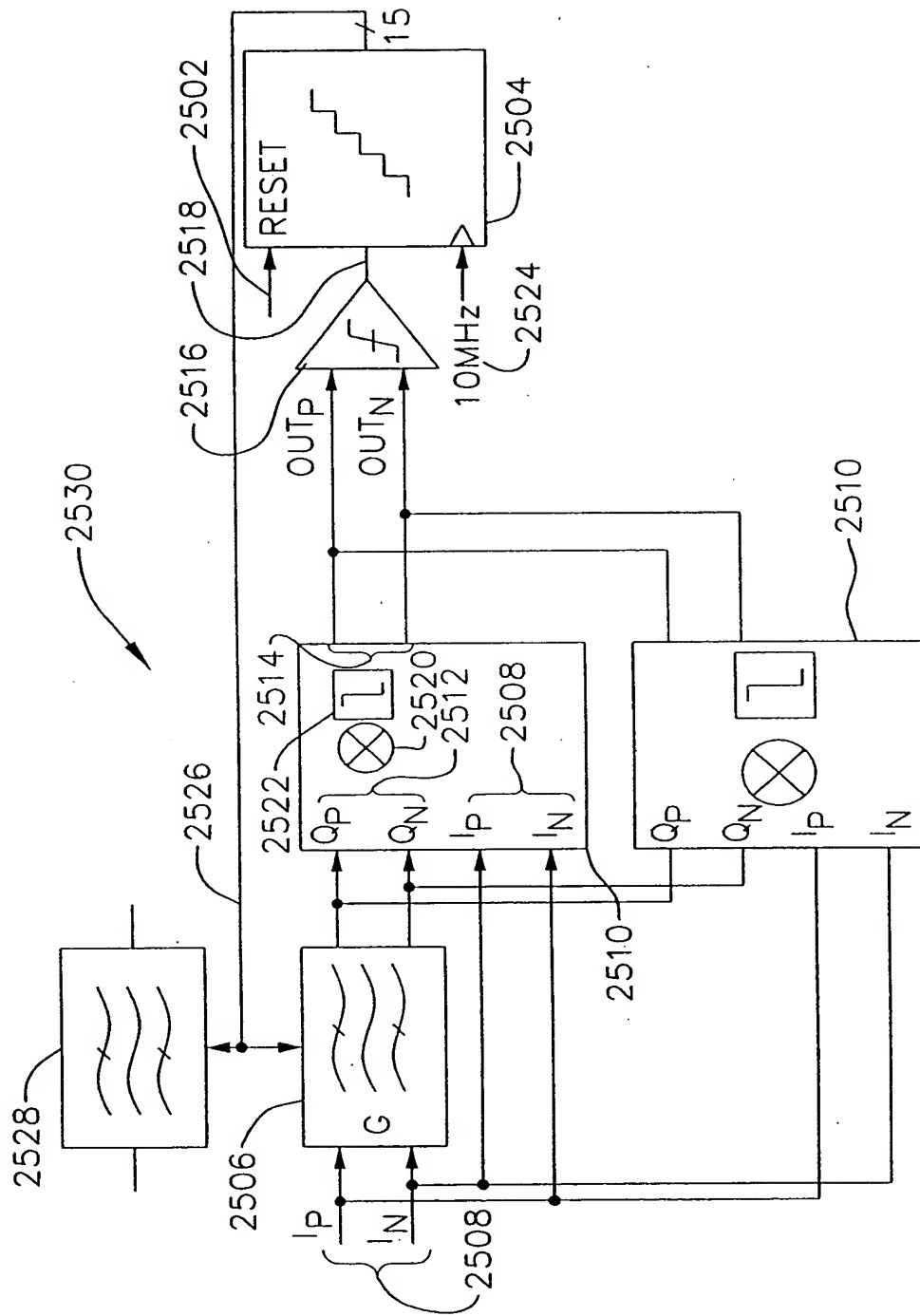


FIG. 25



*FIG. 26*

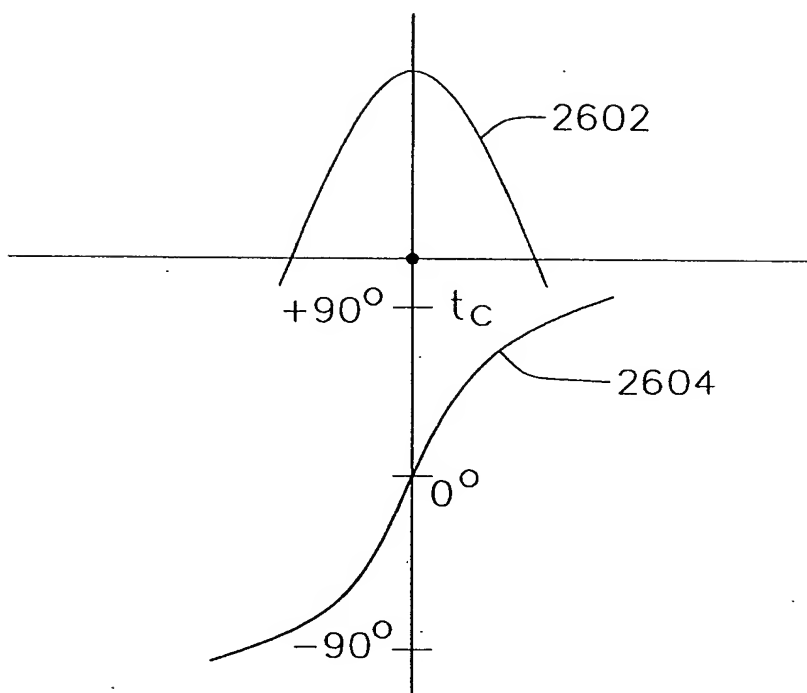
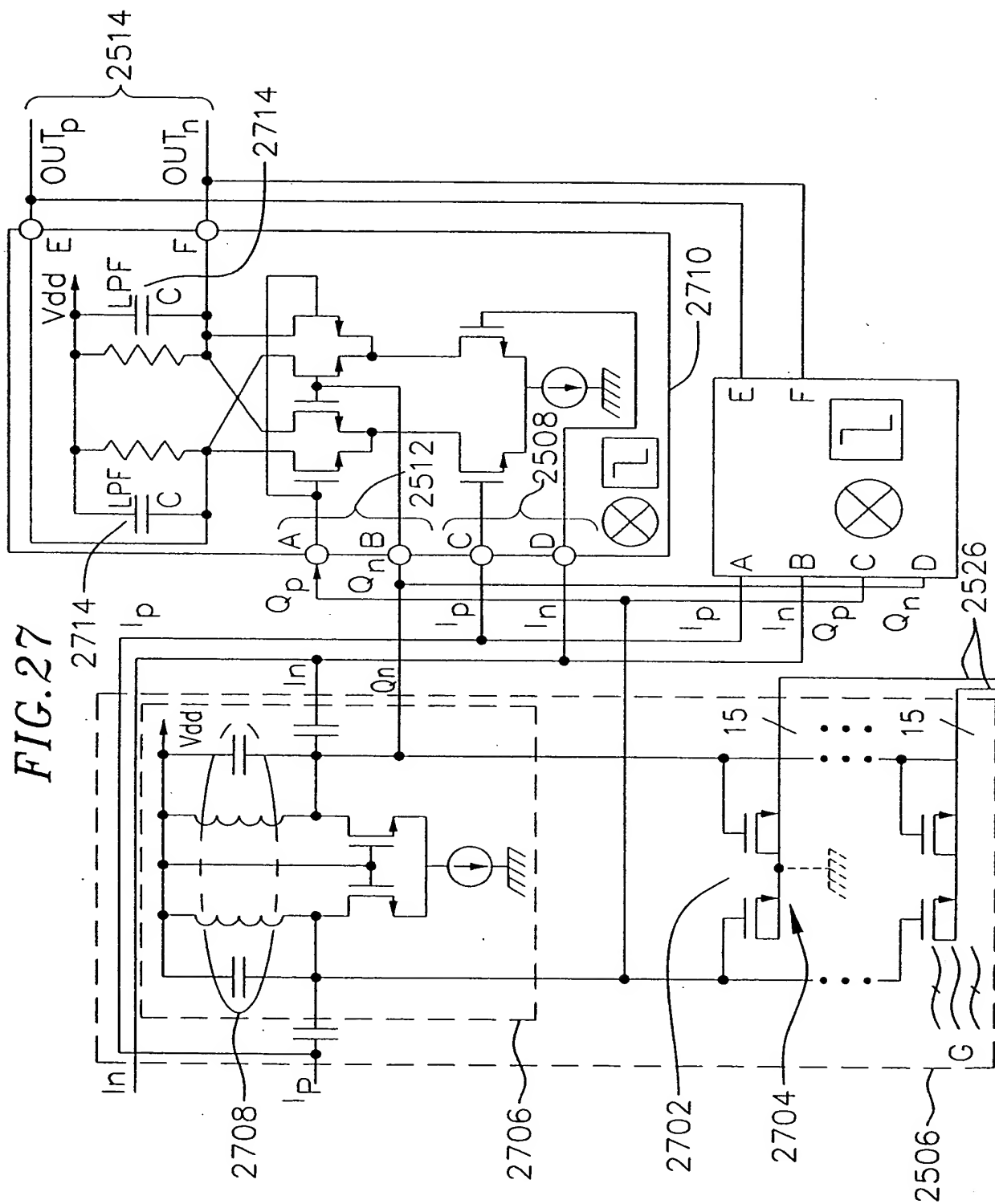
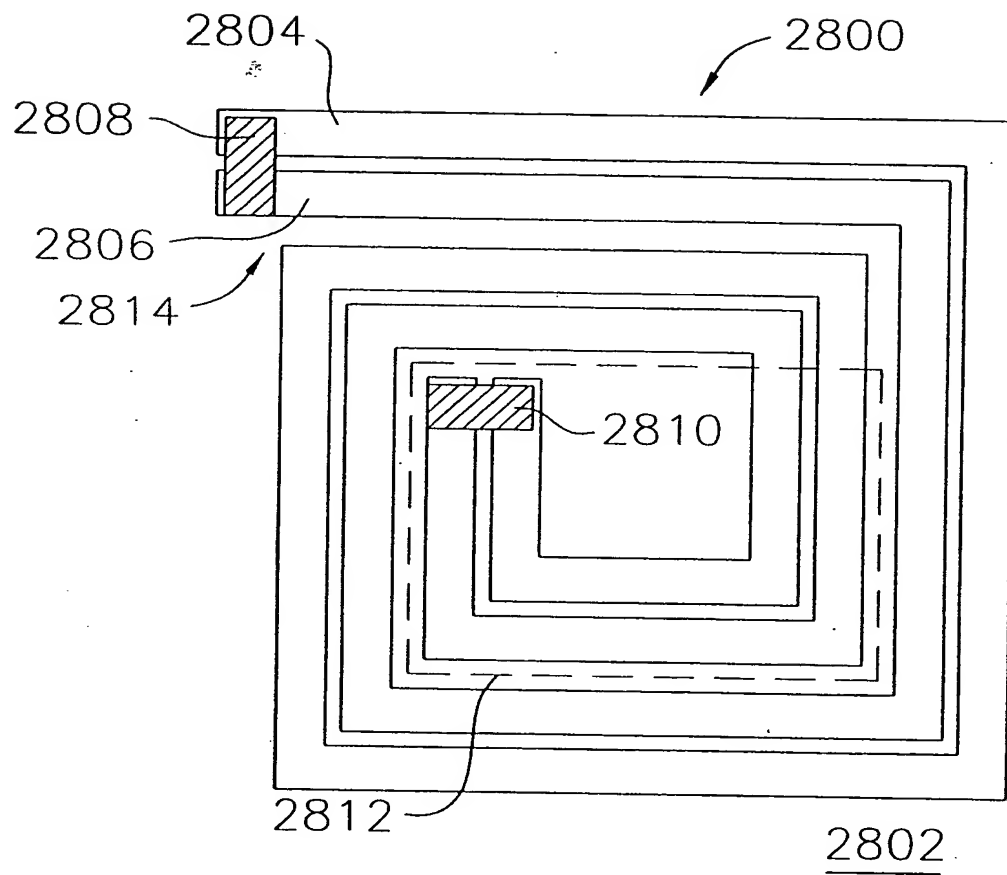


FIG. 27



*FIG. 28a*



**FIG. 28b**

2816

2828

2826

2830

2852

2818

2832

2836

2828

2830

2834

FIG. 28c

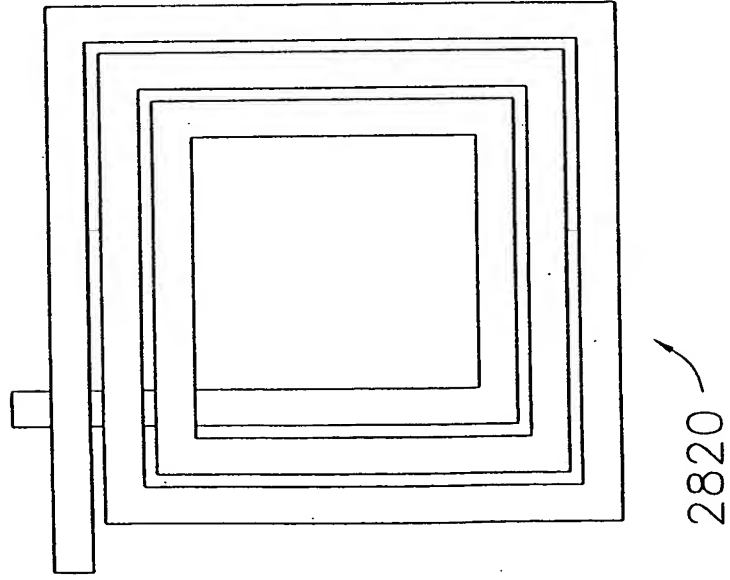


FIG. 28d

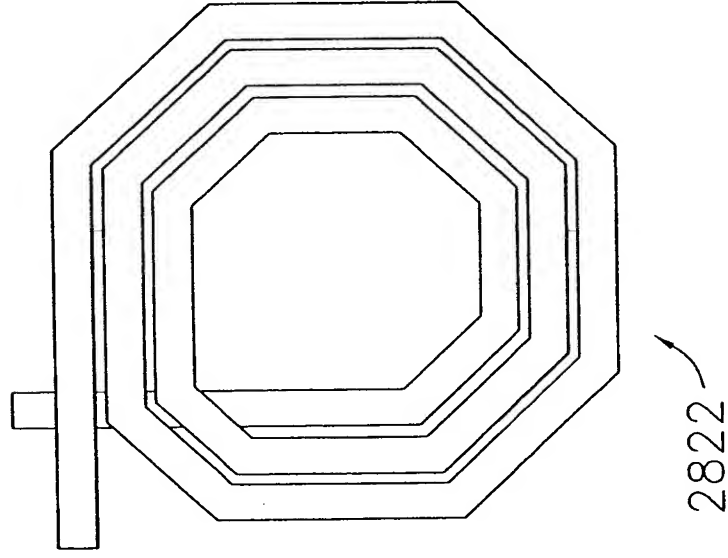
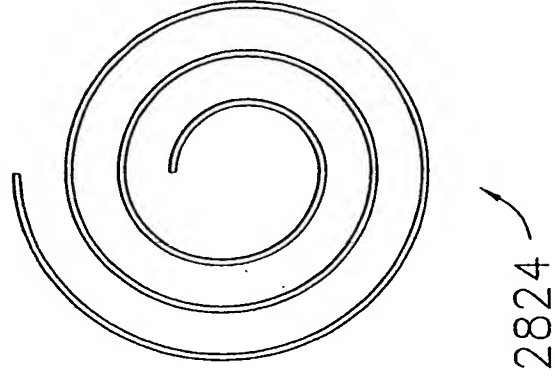
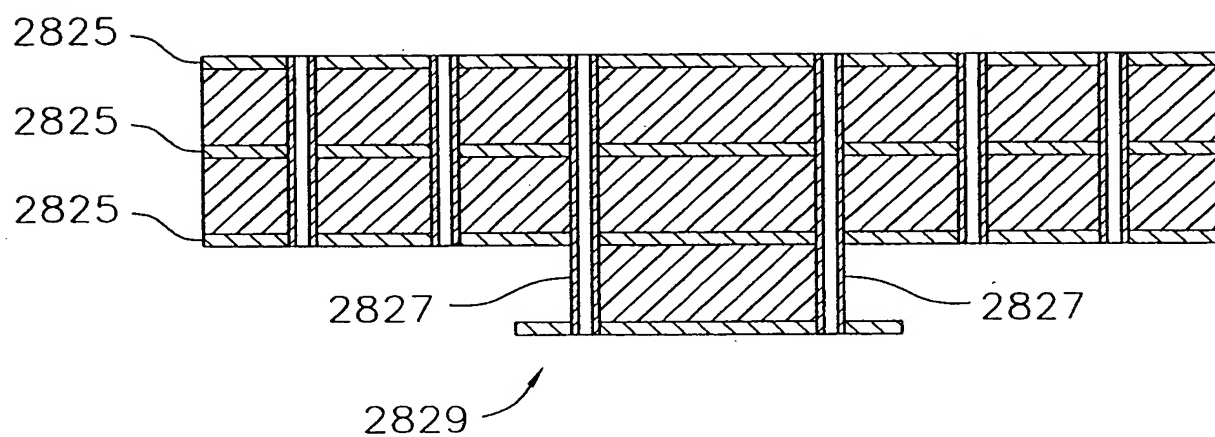


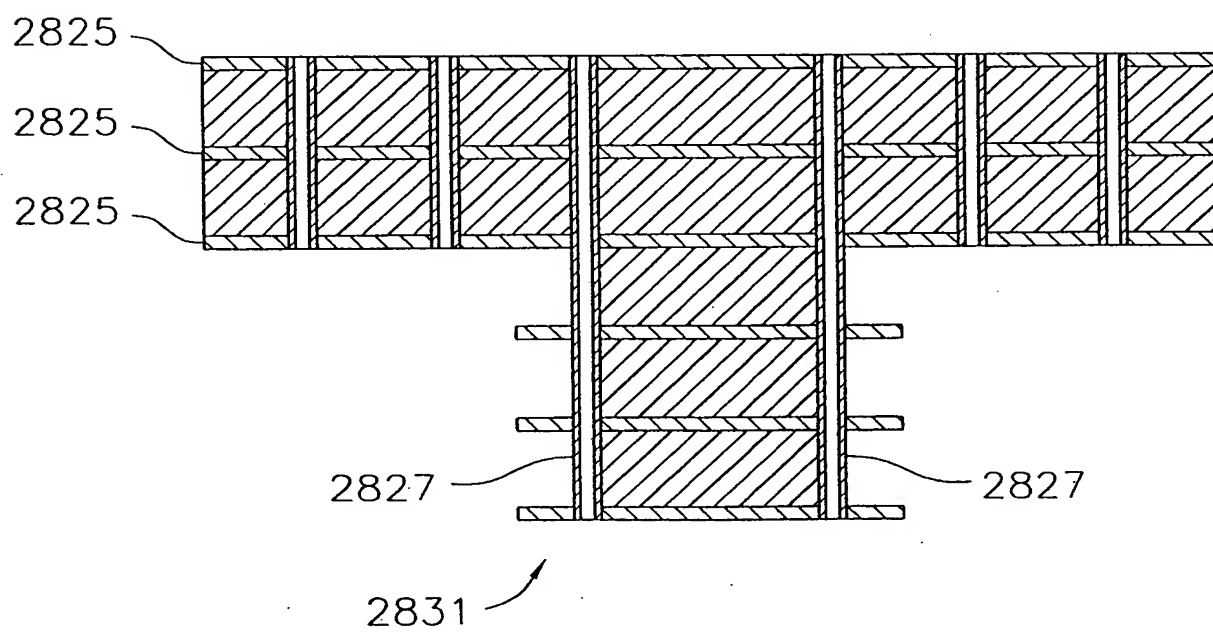
FIG. 28e



*FIG. 28f*



*FIG. 28g*



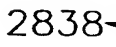


FIG. 28i

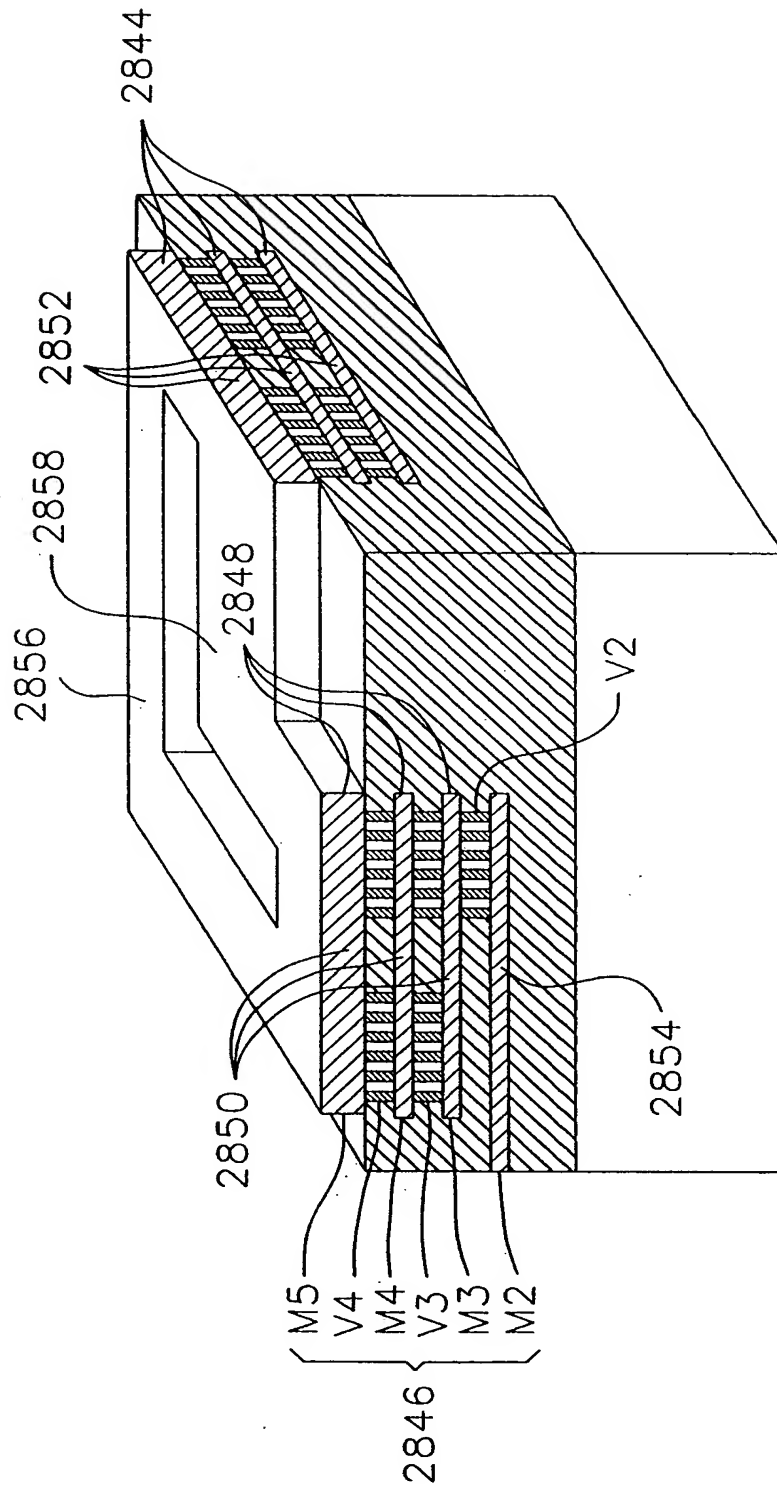


FIG. 28j

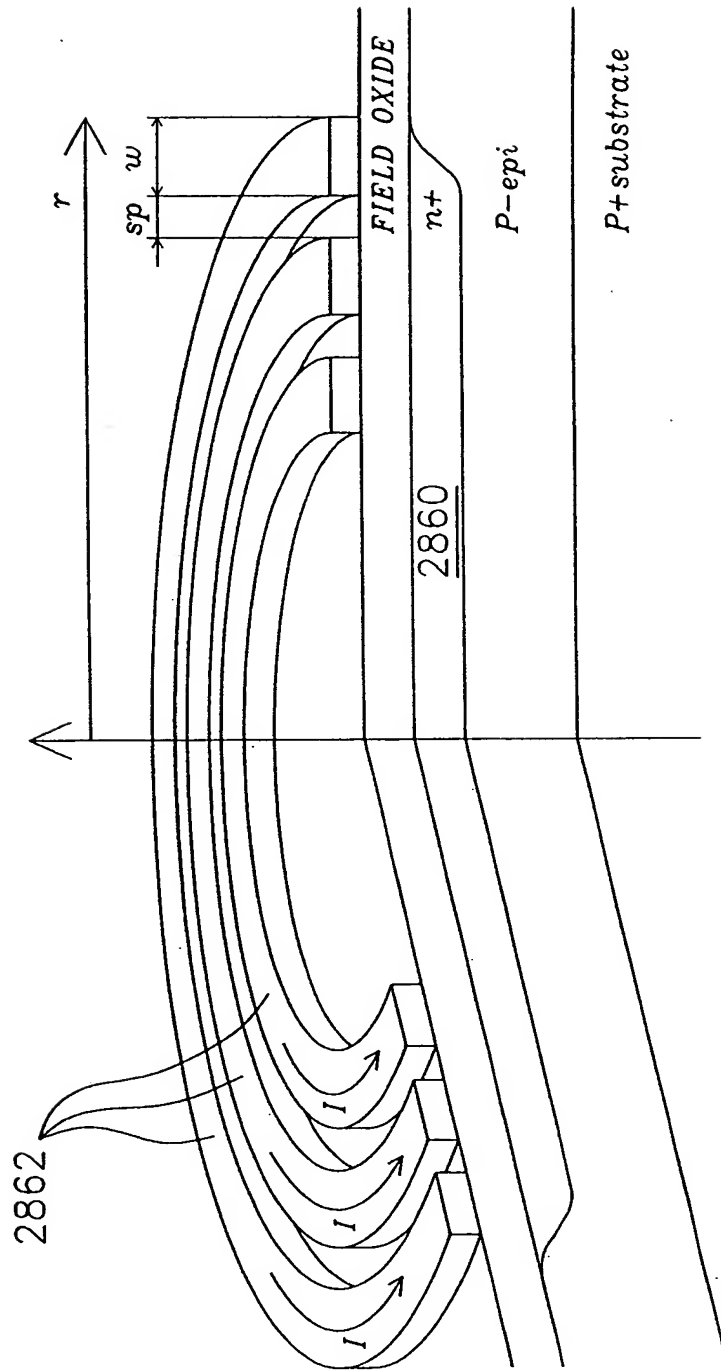
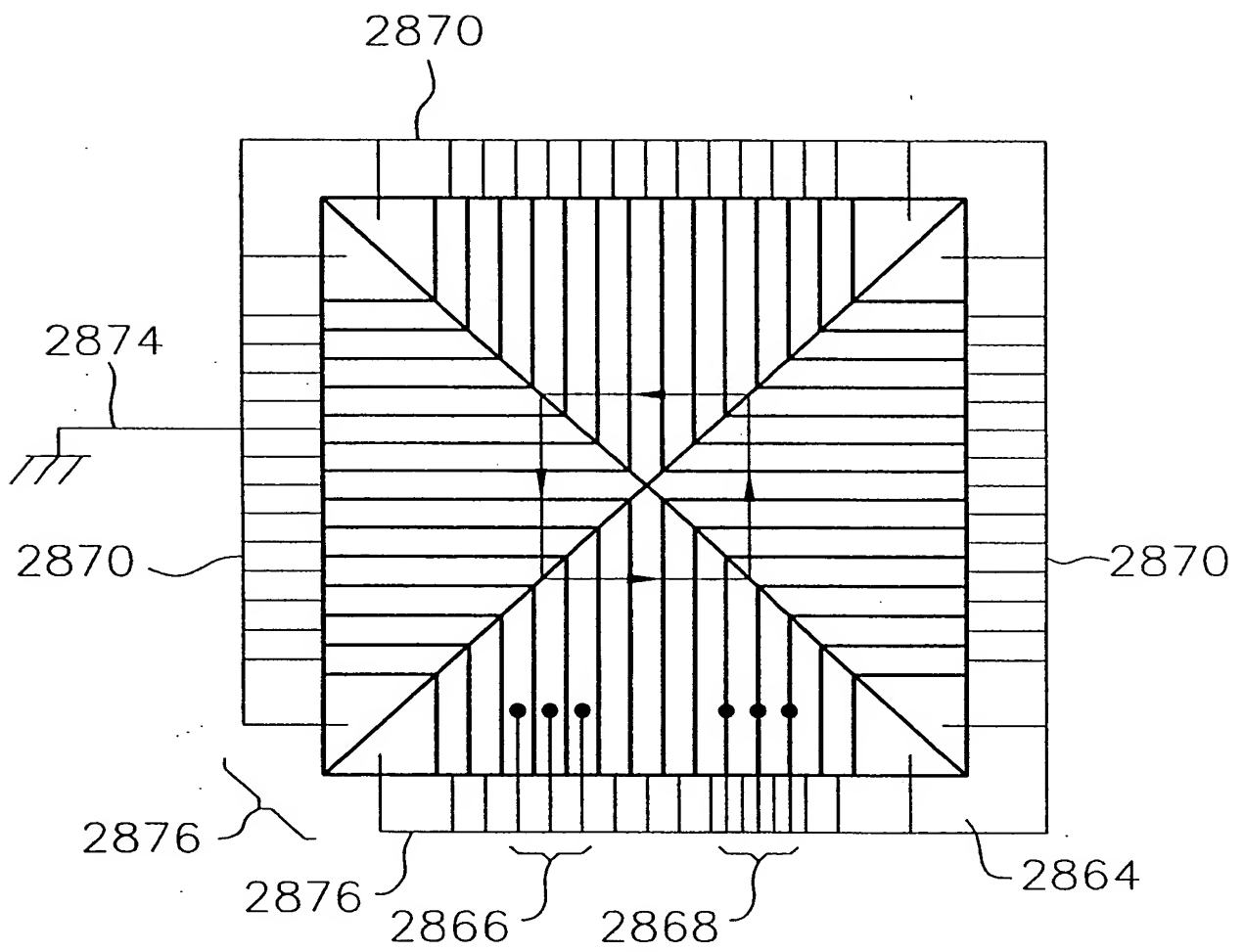


FIG. 28k



*FIG.29*

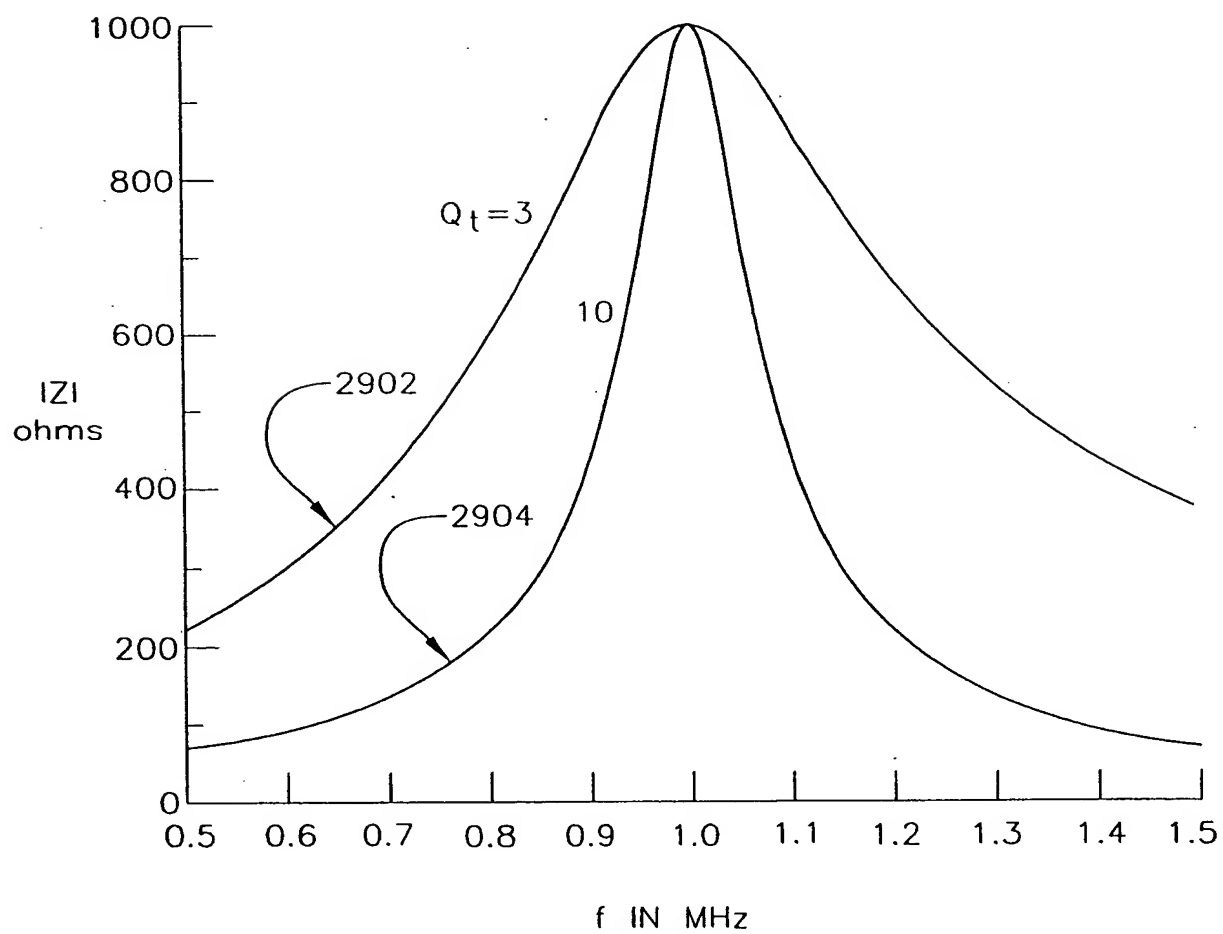


FIG. 30

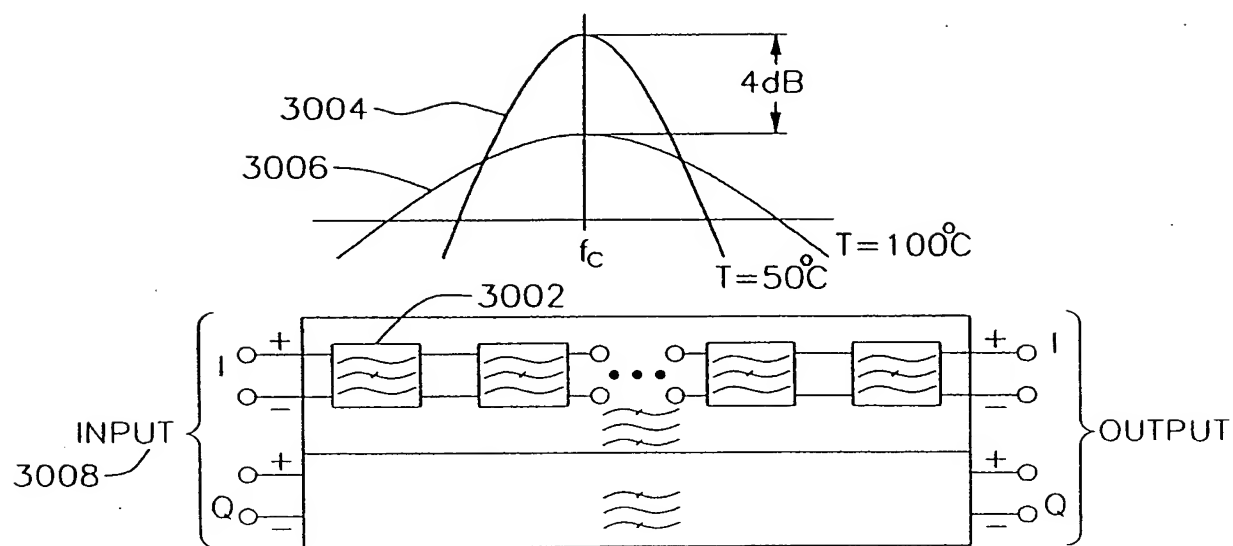


FIG. 31A

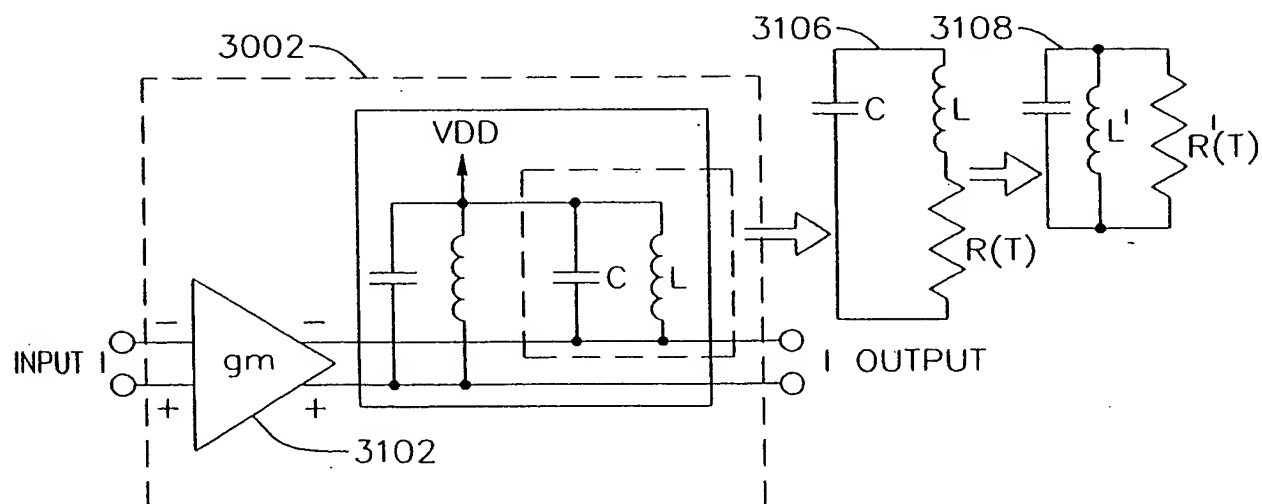


FIG. 31B

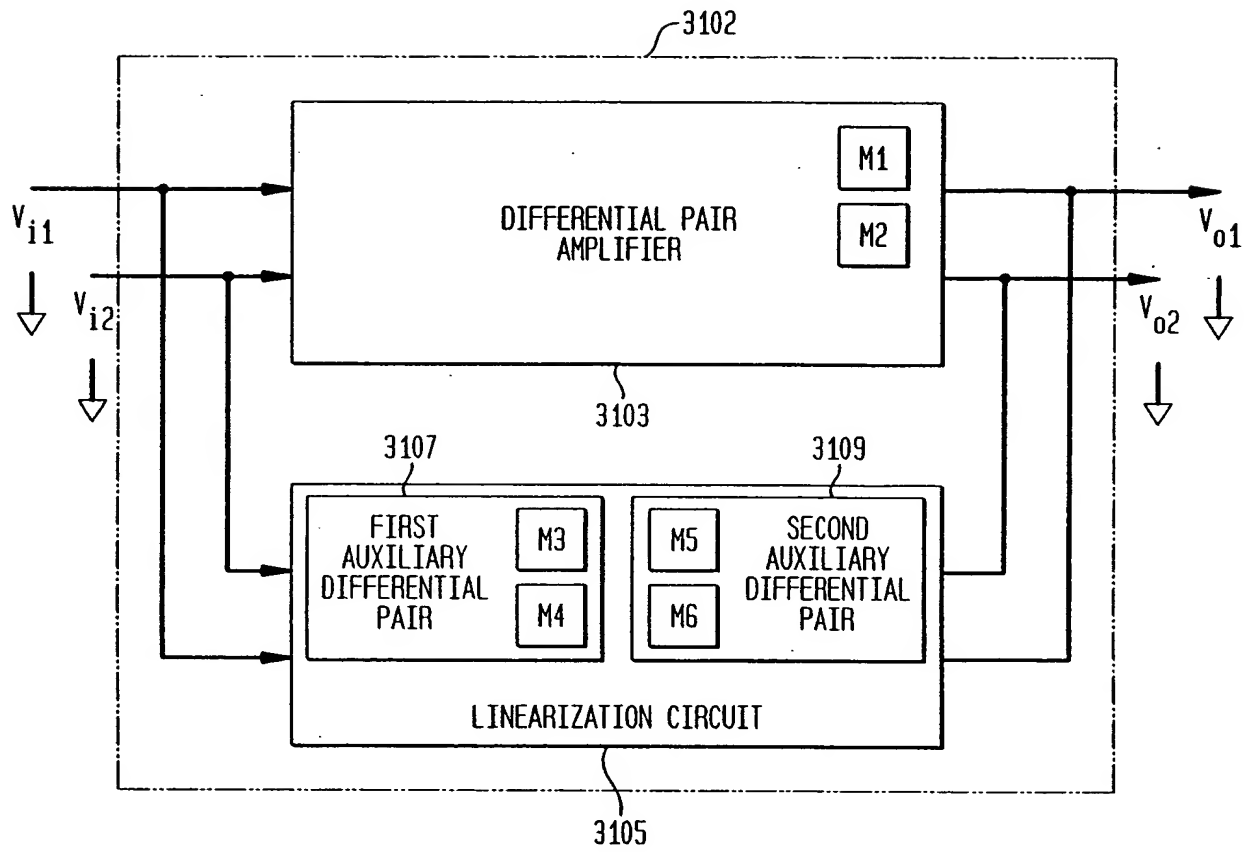


FIG. 31C

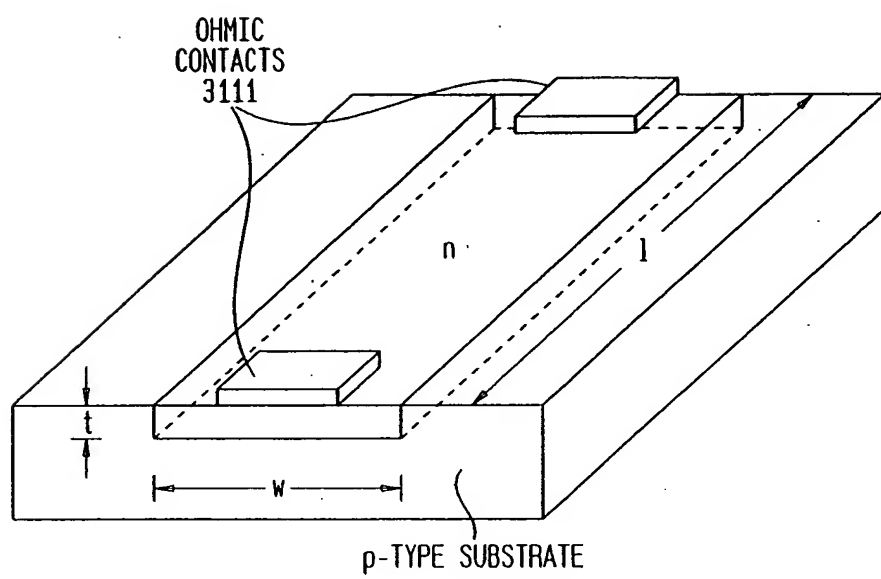


FIG. 31D

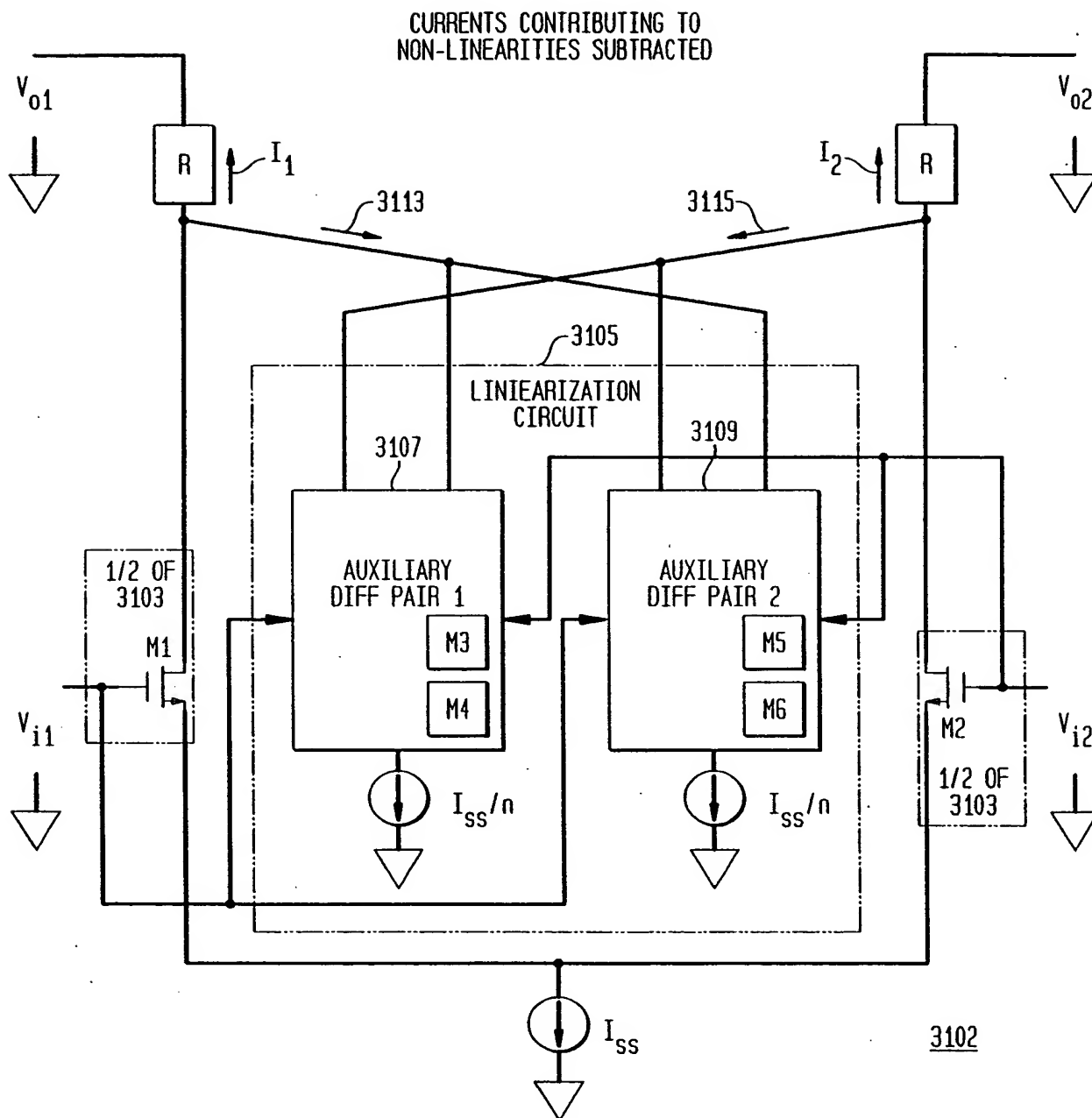


FIG. 31E

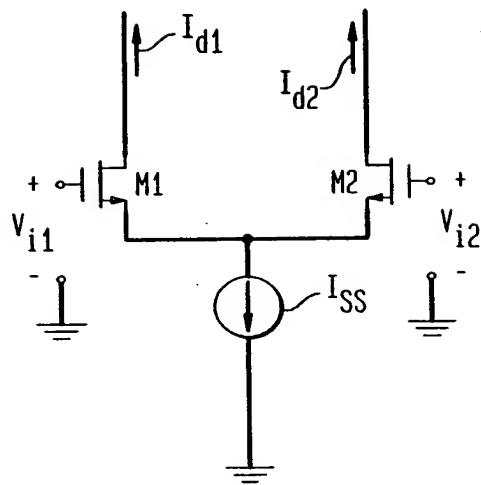


FIG. 31F

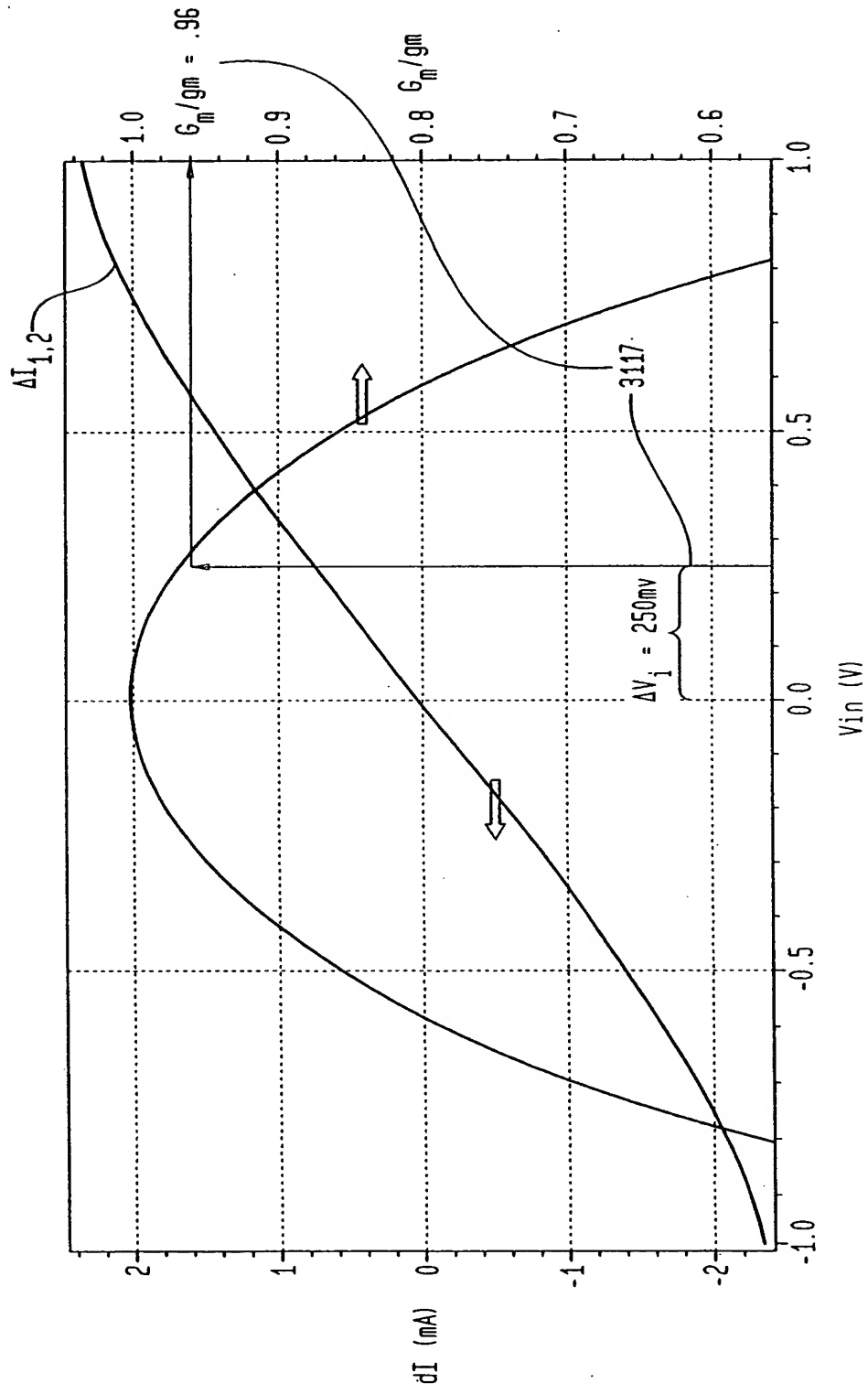


FIG. 316

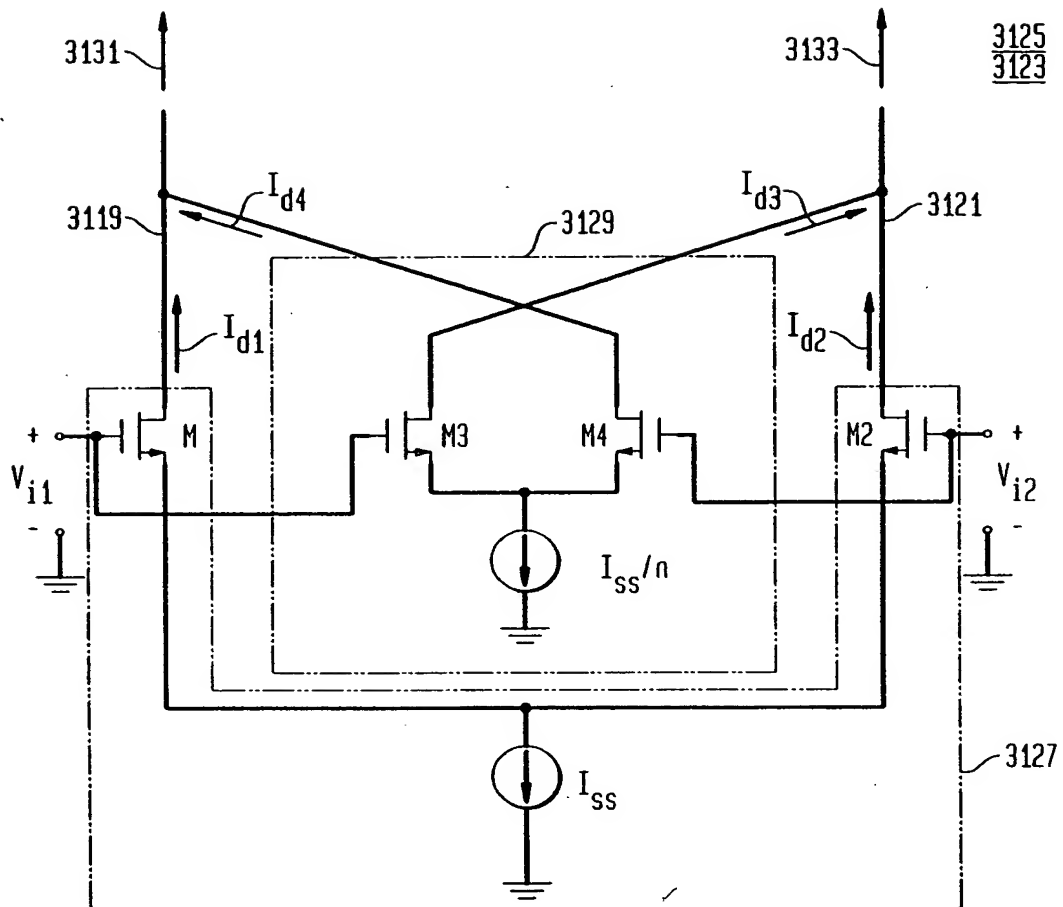


FIG. 31H

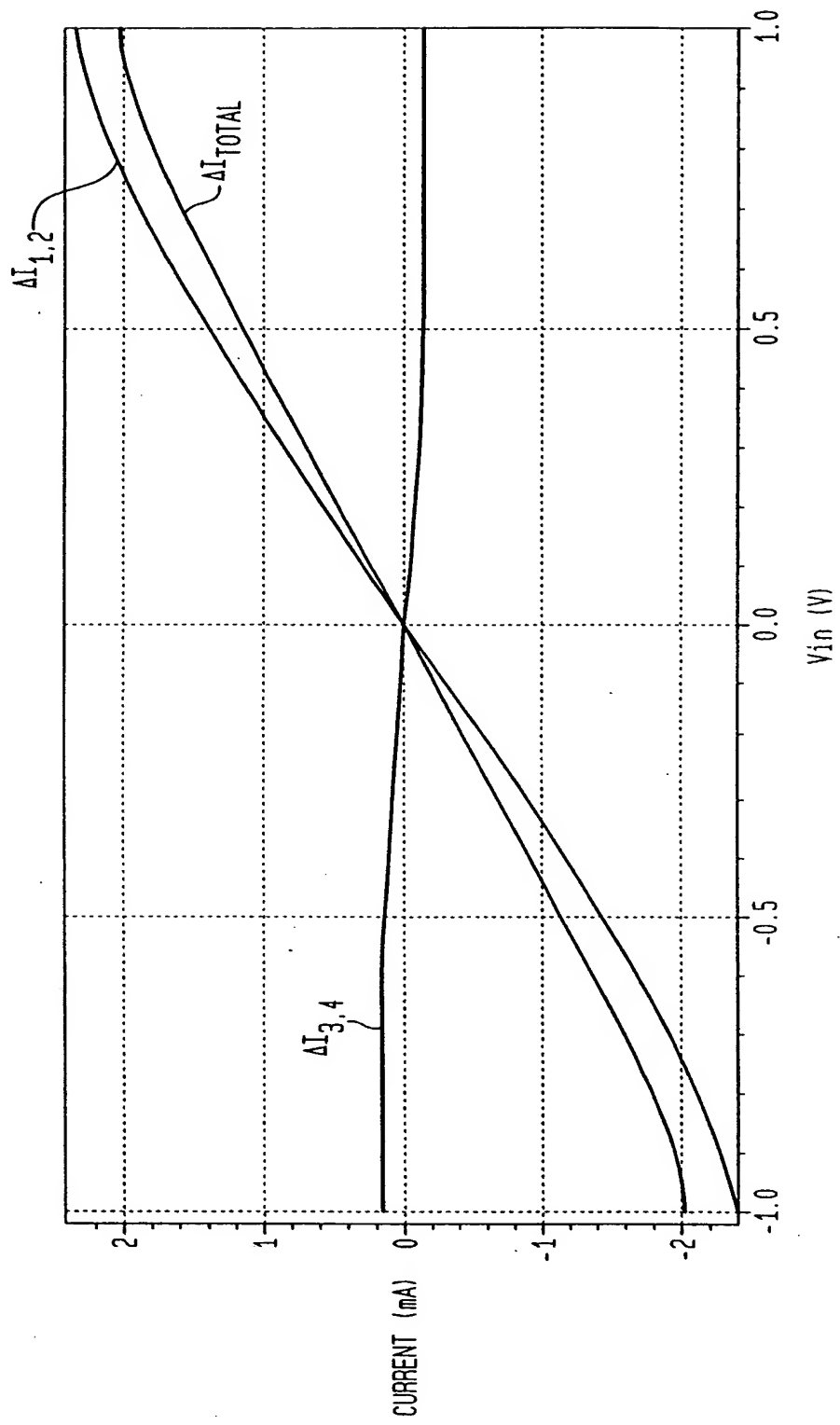


FIG. 31I

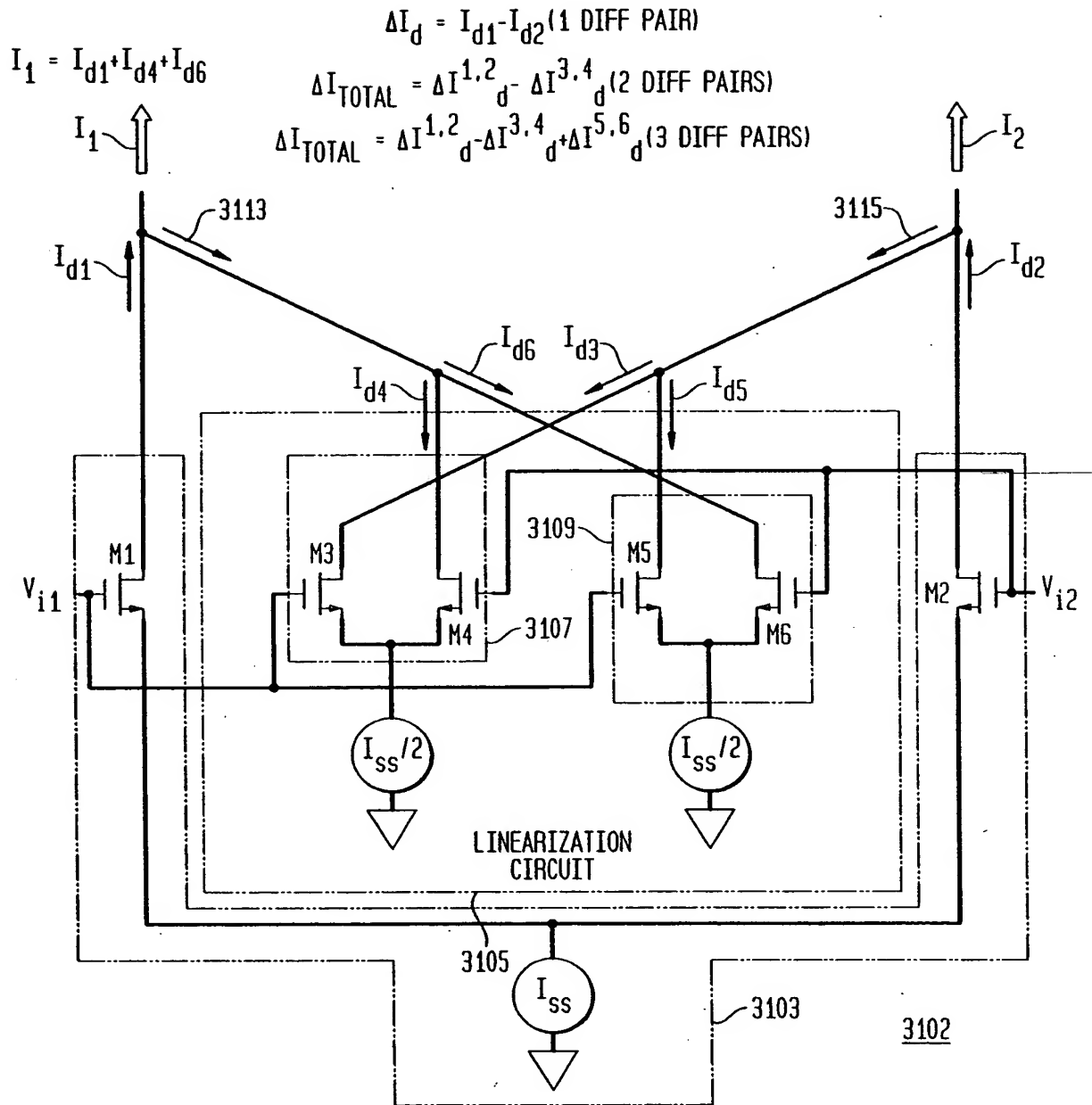


FIG. 31J

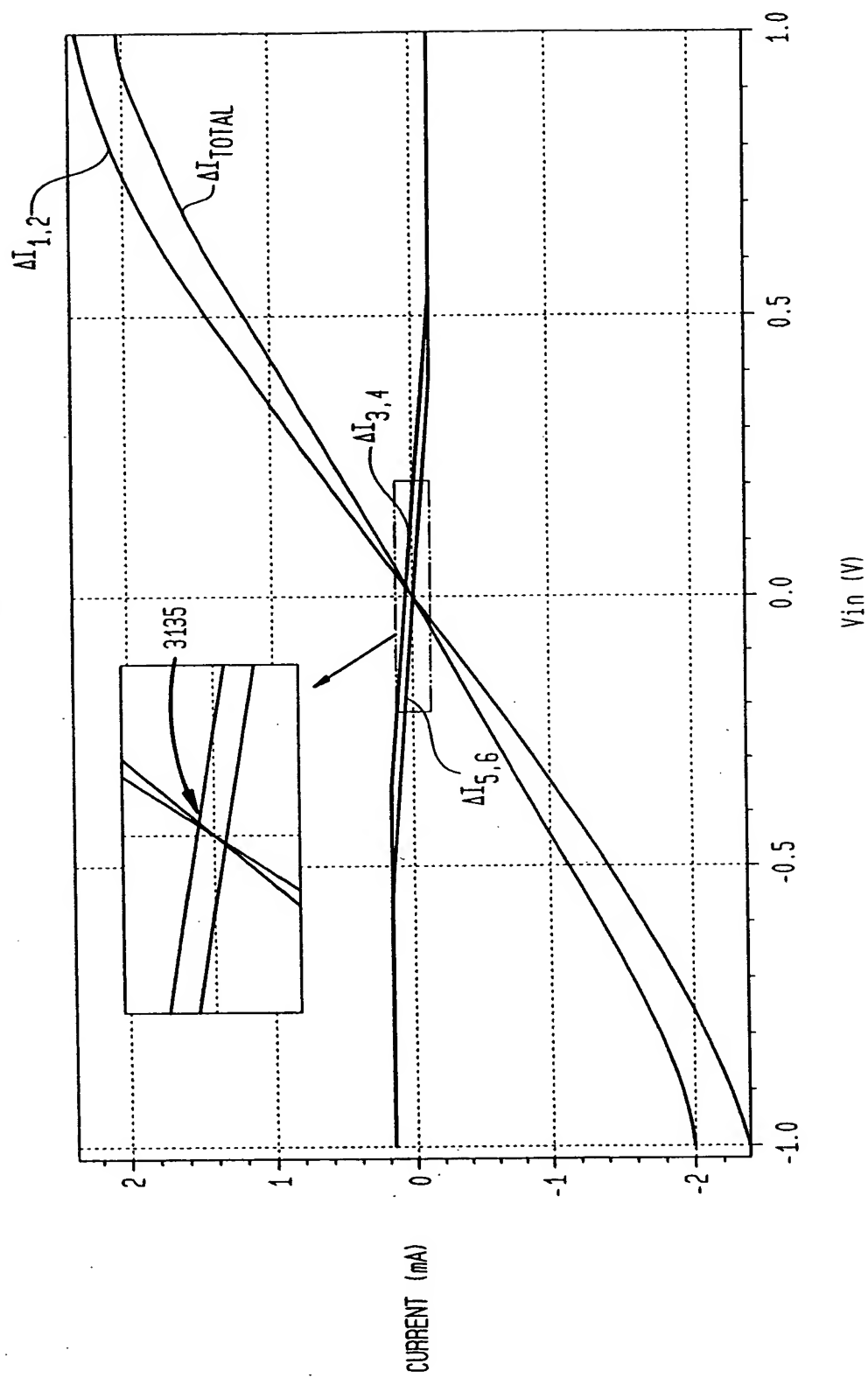


FIG. 31K

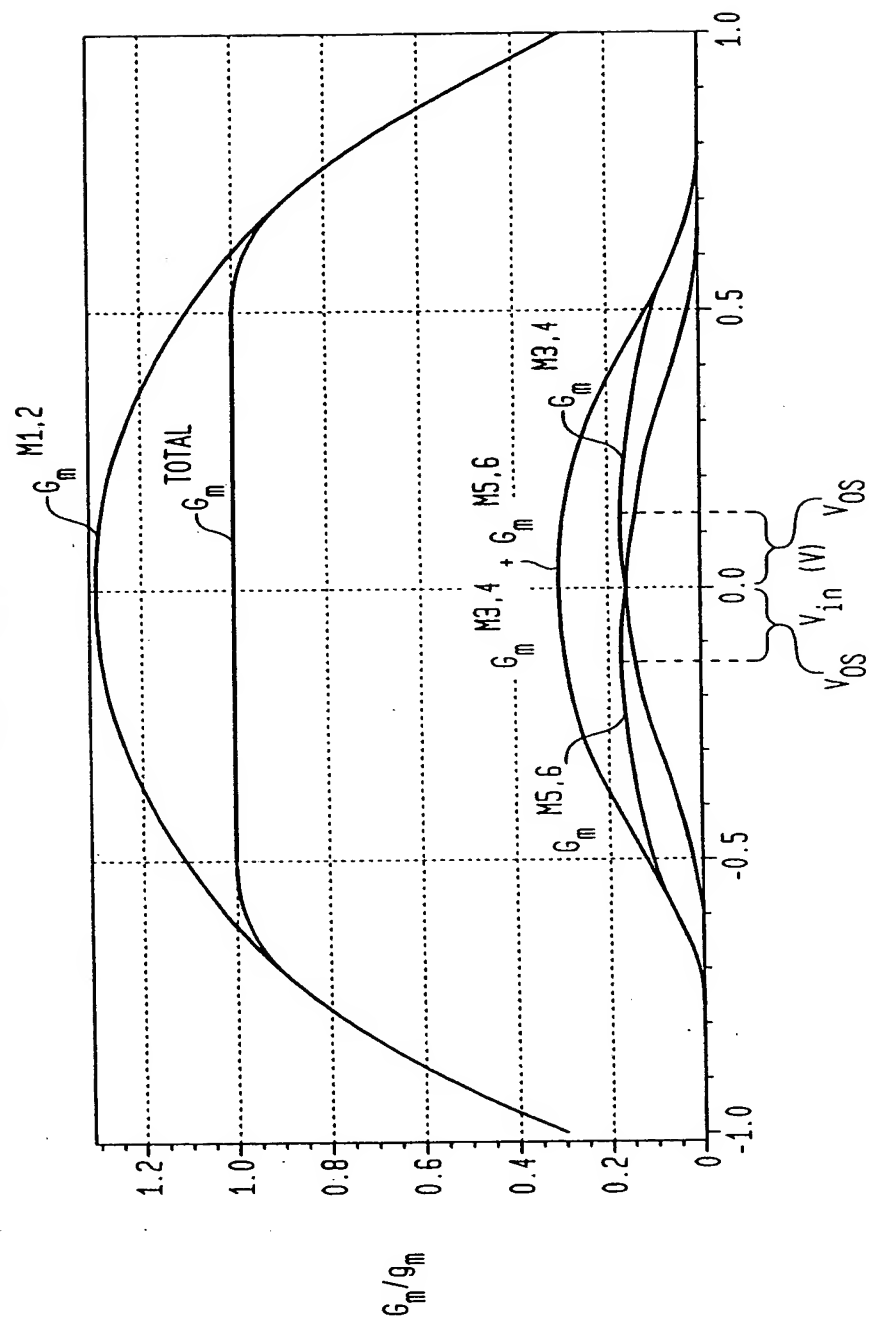


FIG. 31L

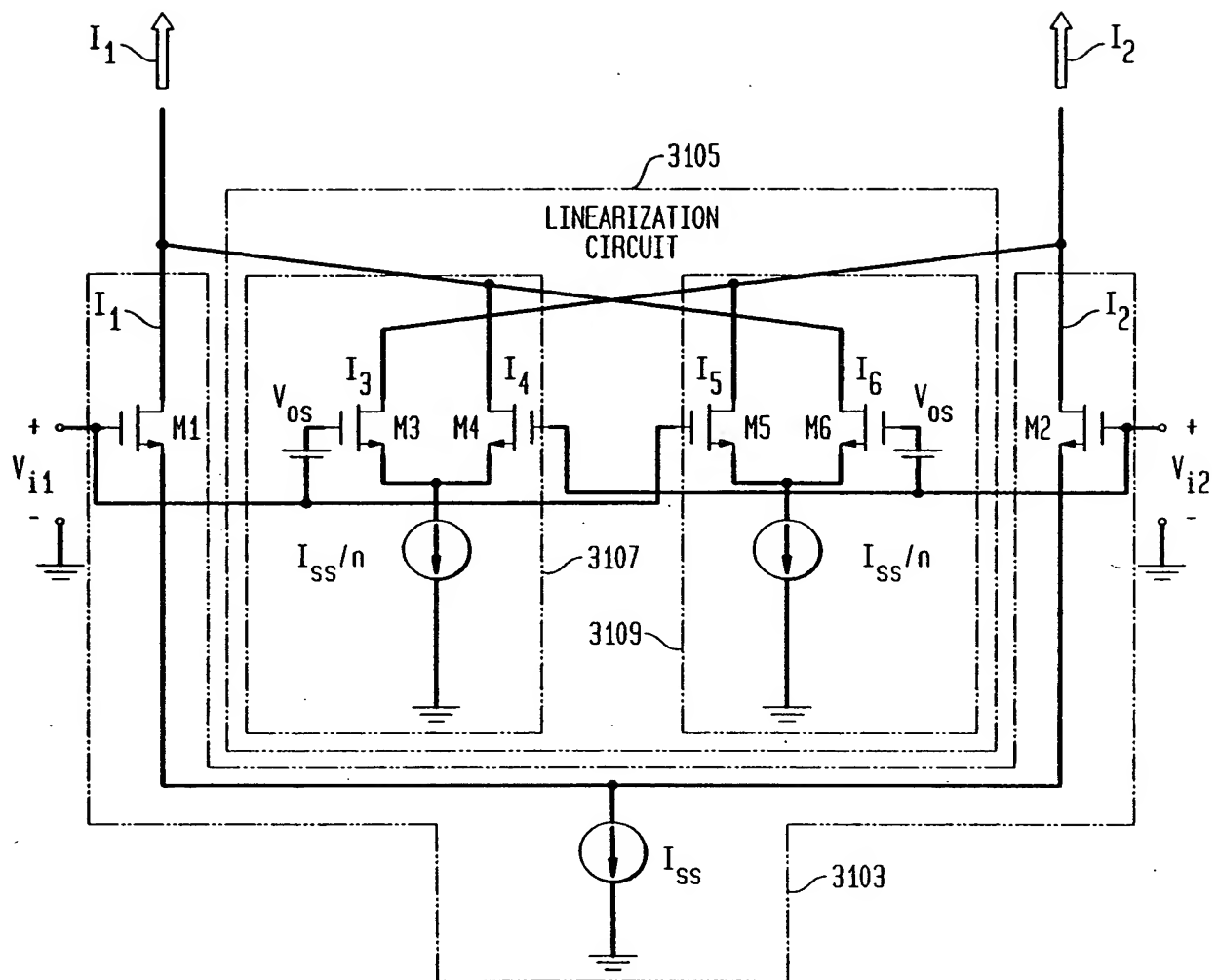


FIG. 31M

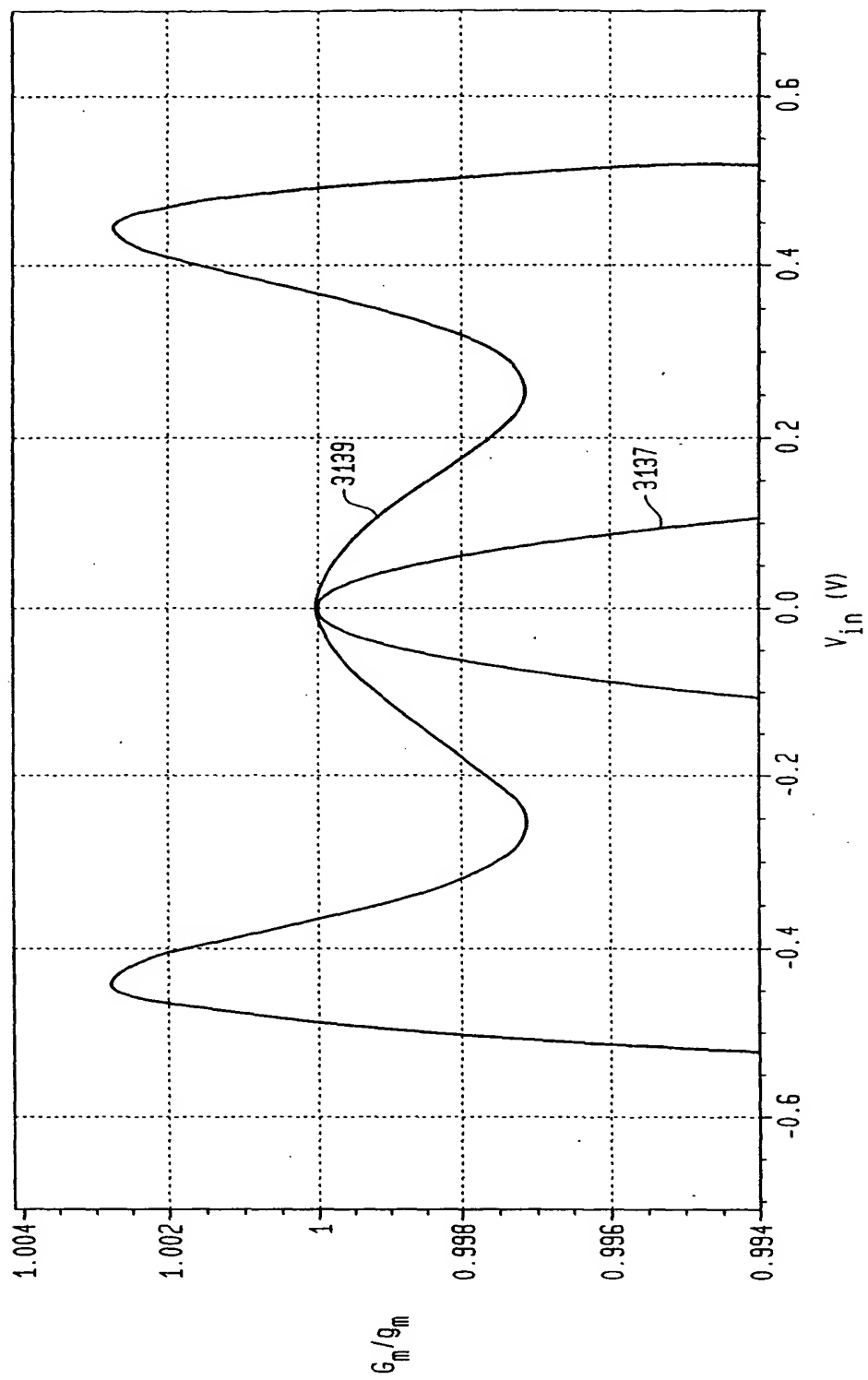
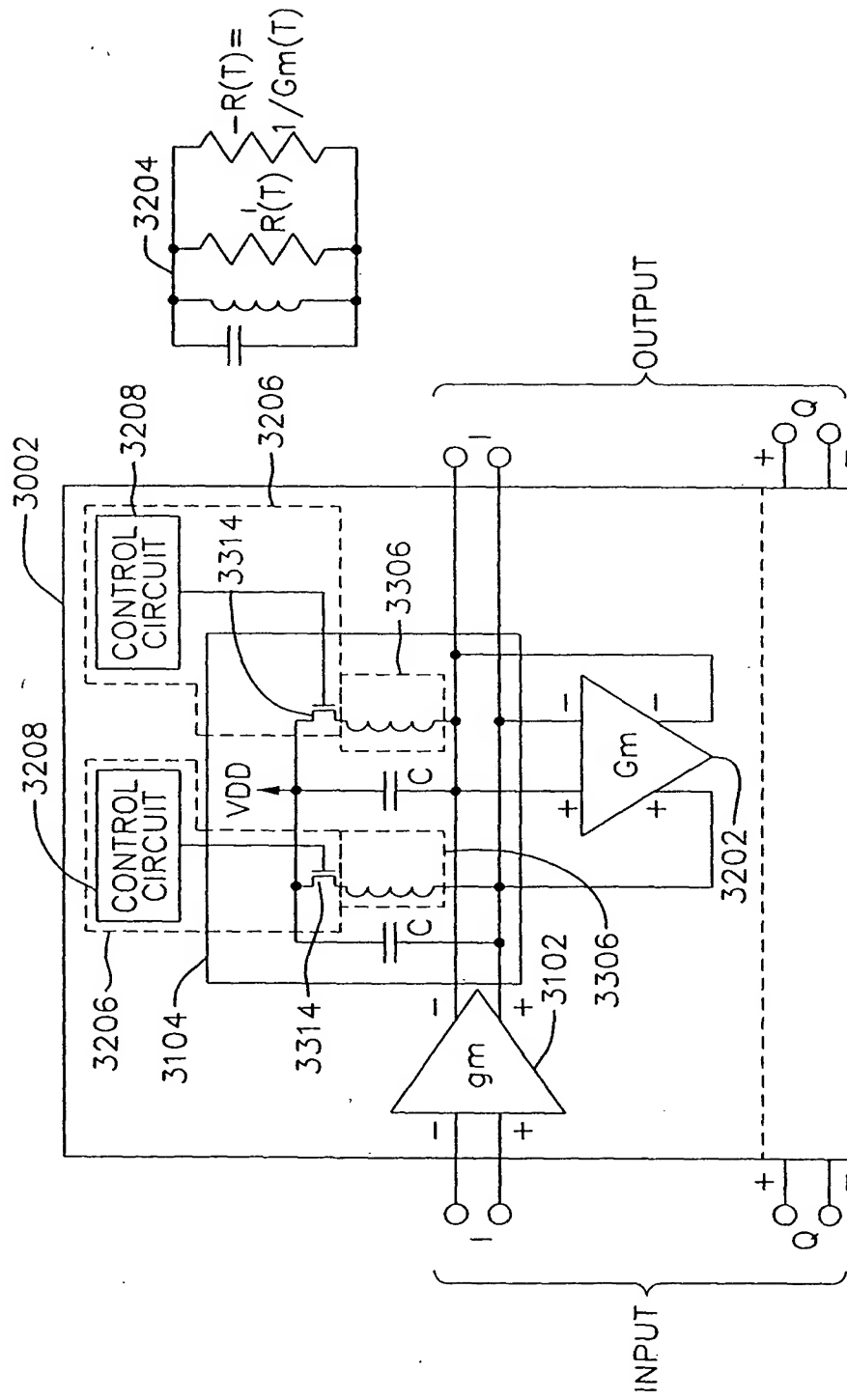


FIG. 32



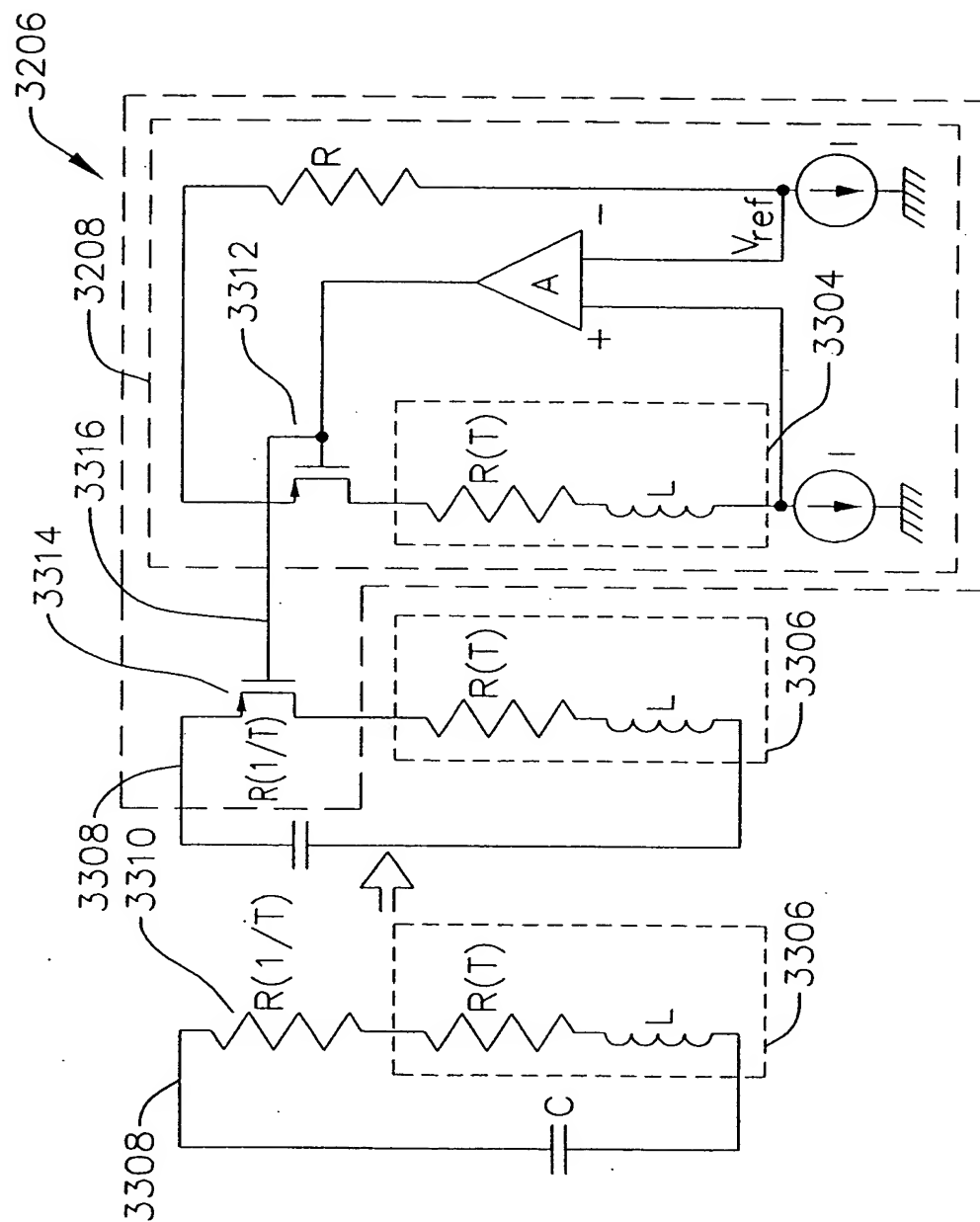
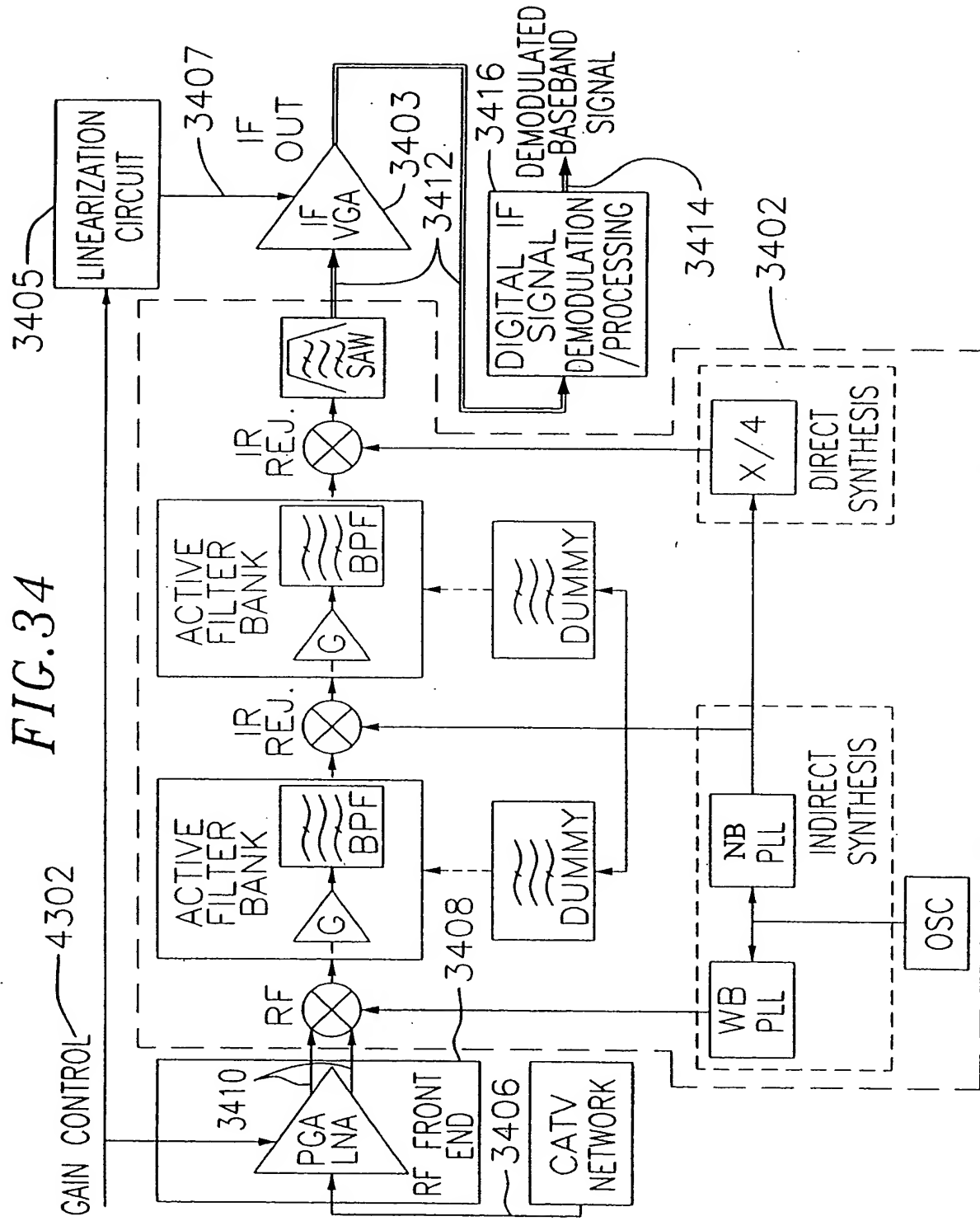


FIG. 34



**FIG. 35**

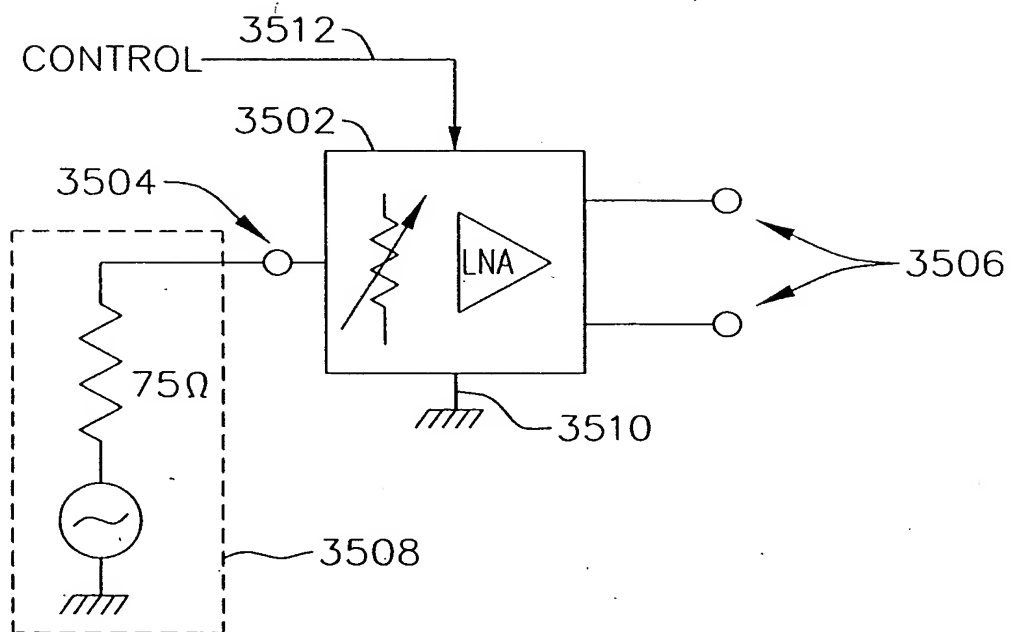


FIG. 36

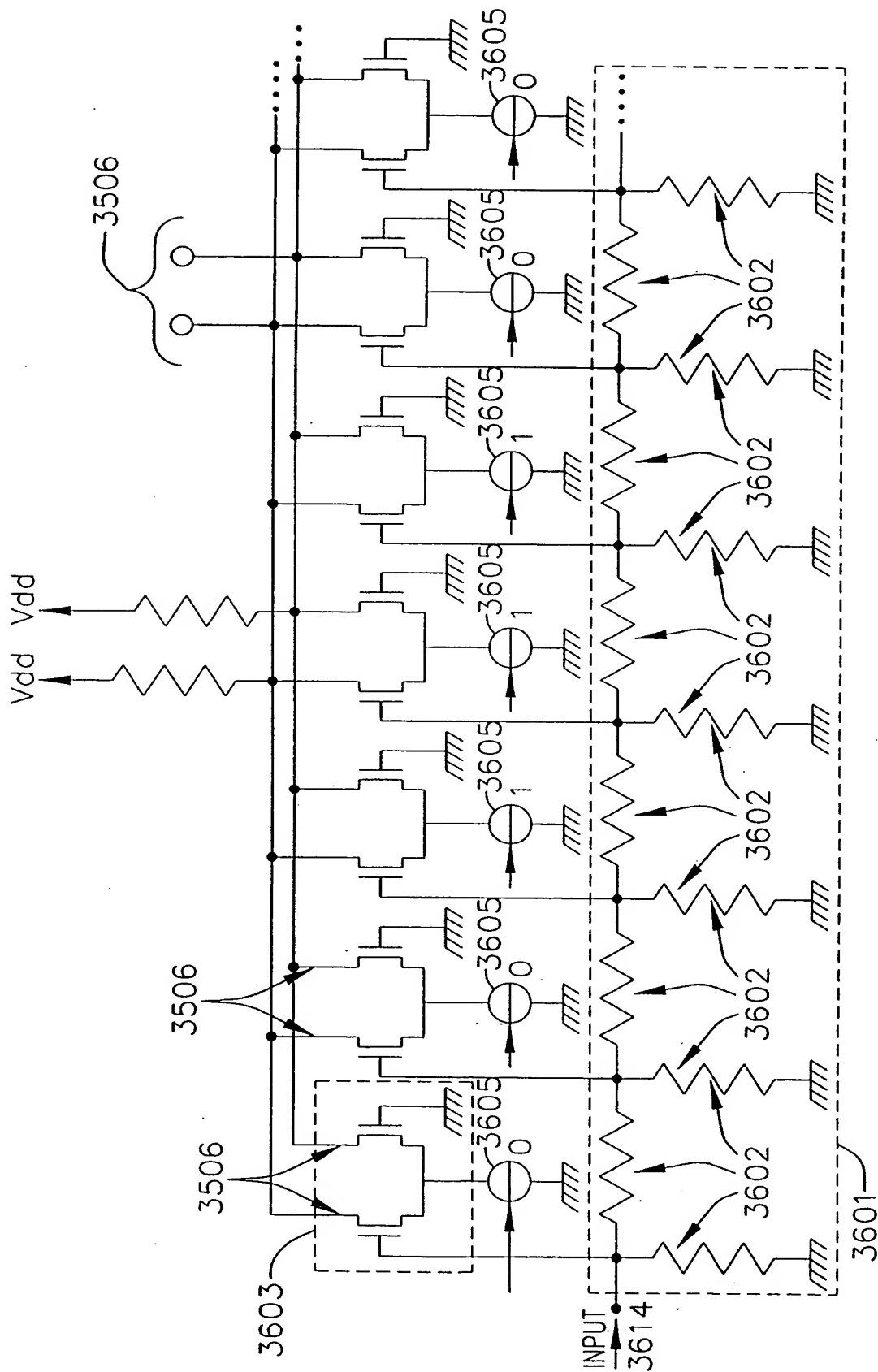


FIG. 37

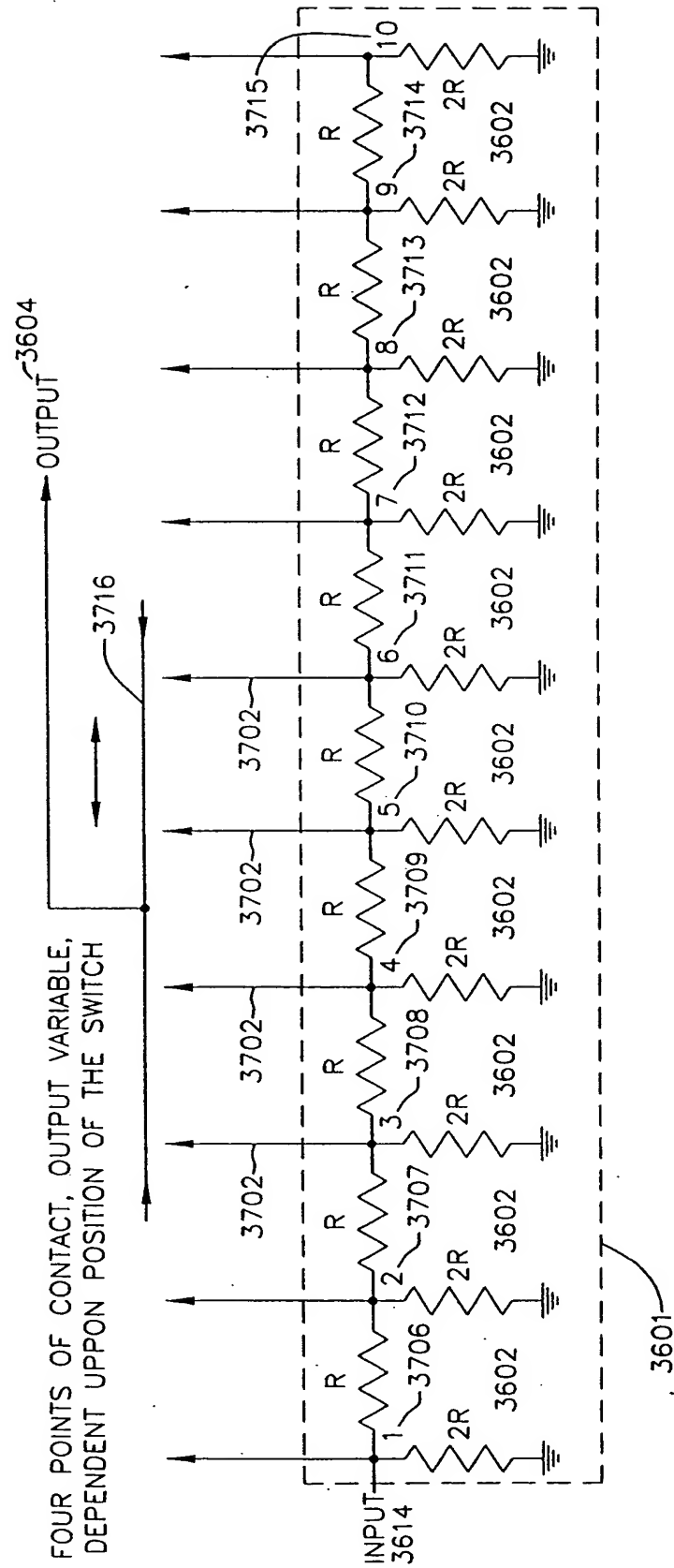


FIG. 38

PGA SETTINGS

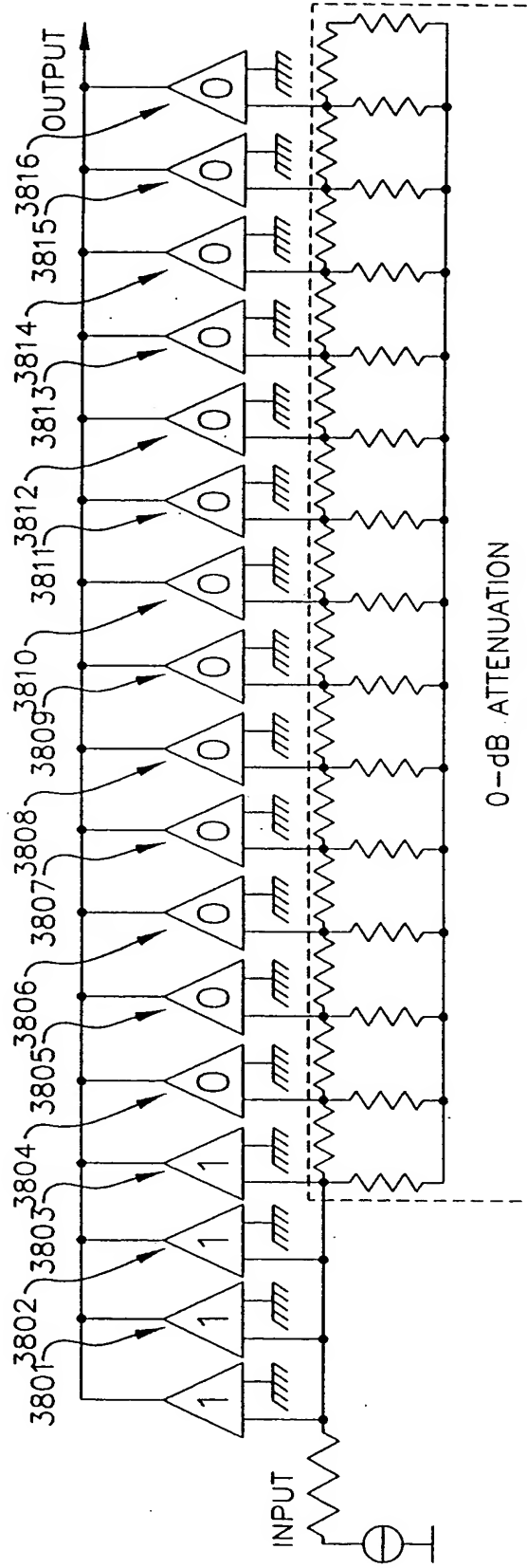


FIG. 39

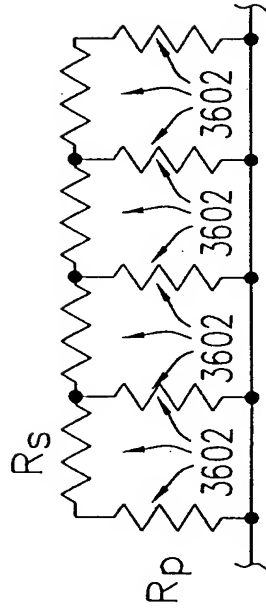


FIG. 40

PGA ARCHITECTURE

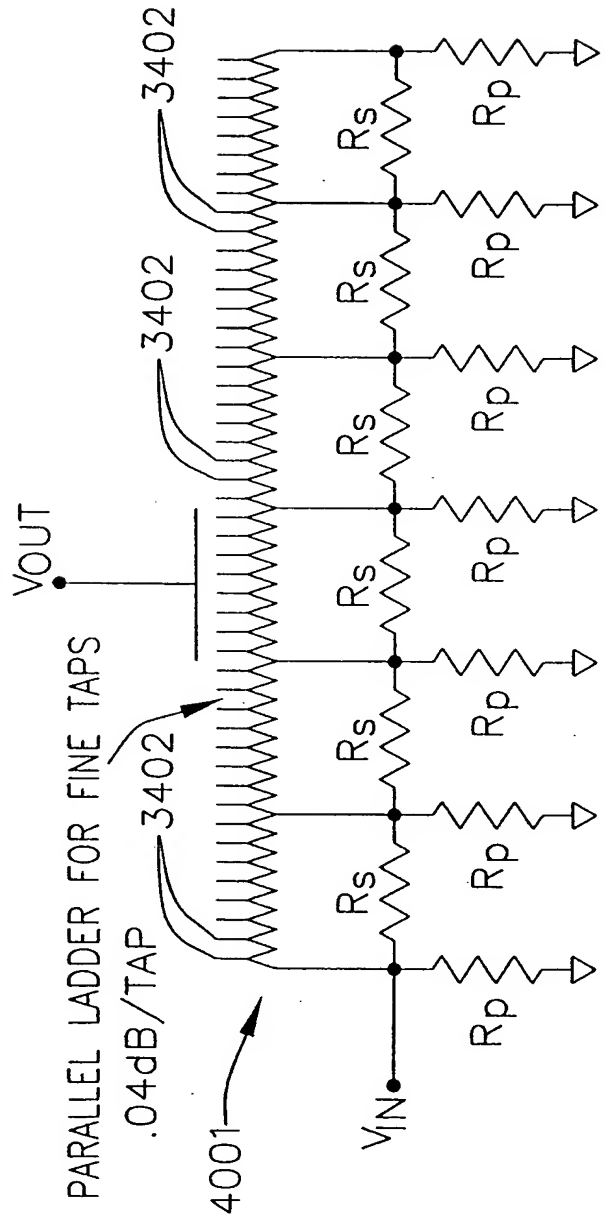


FIG. 41

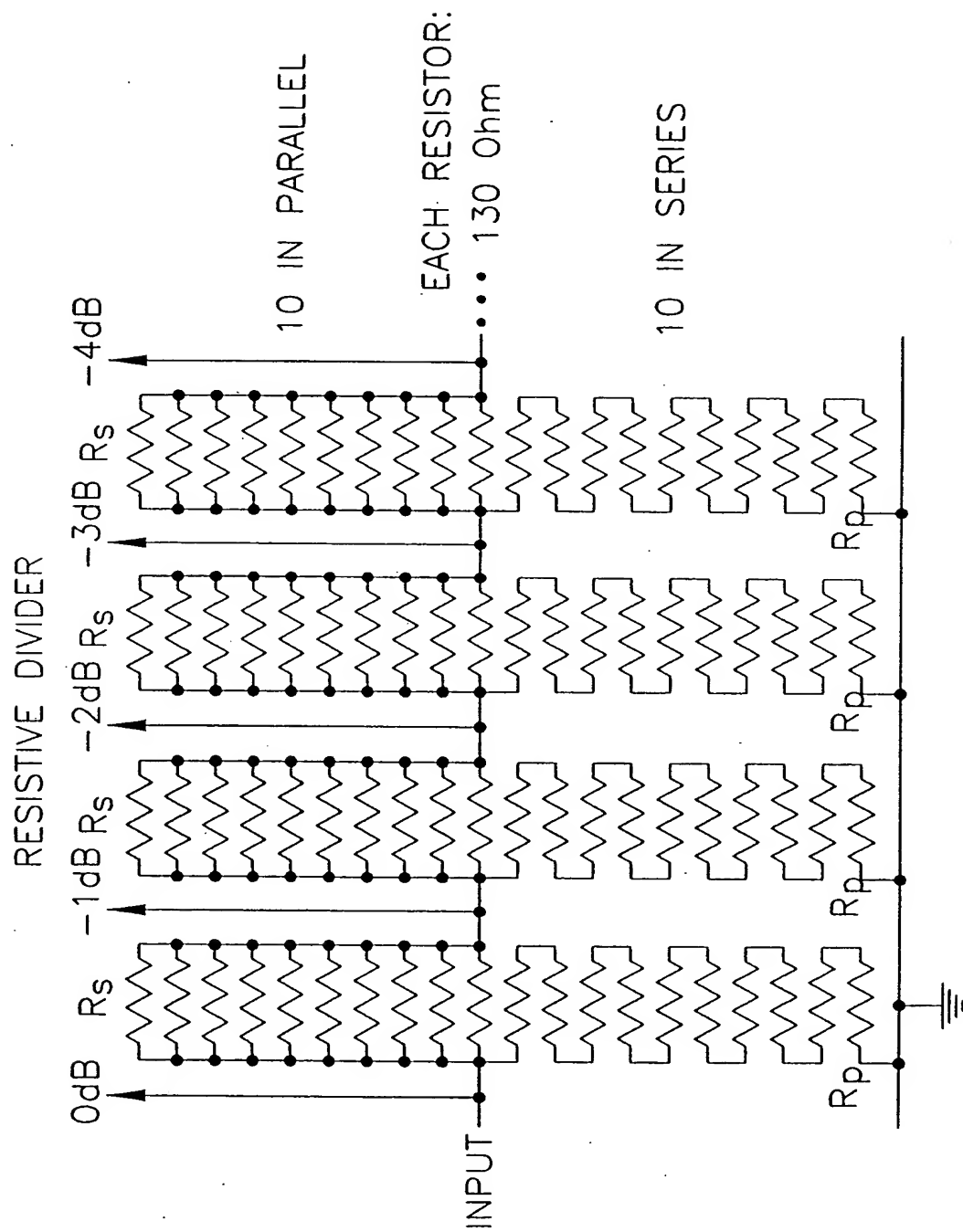
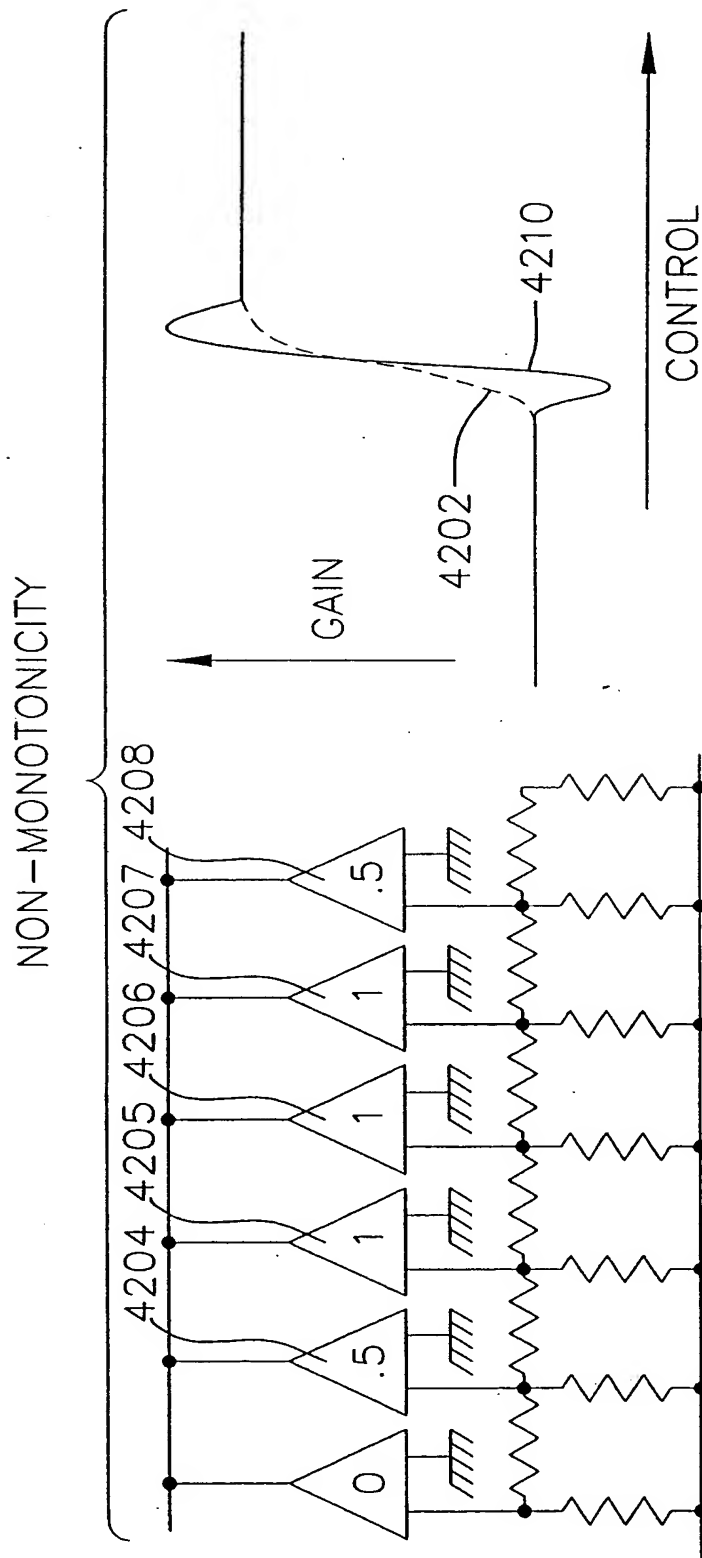
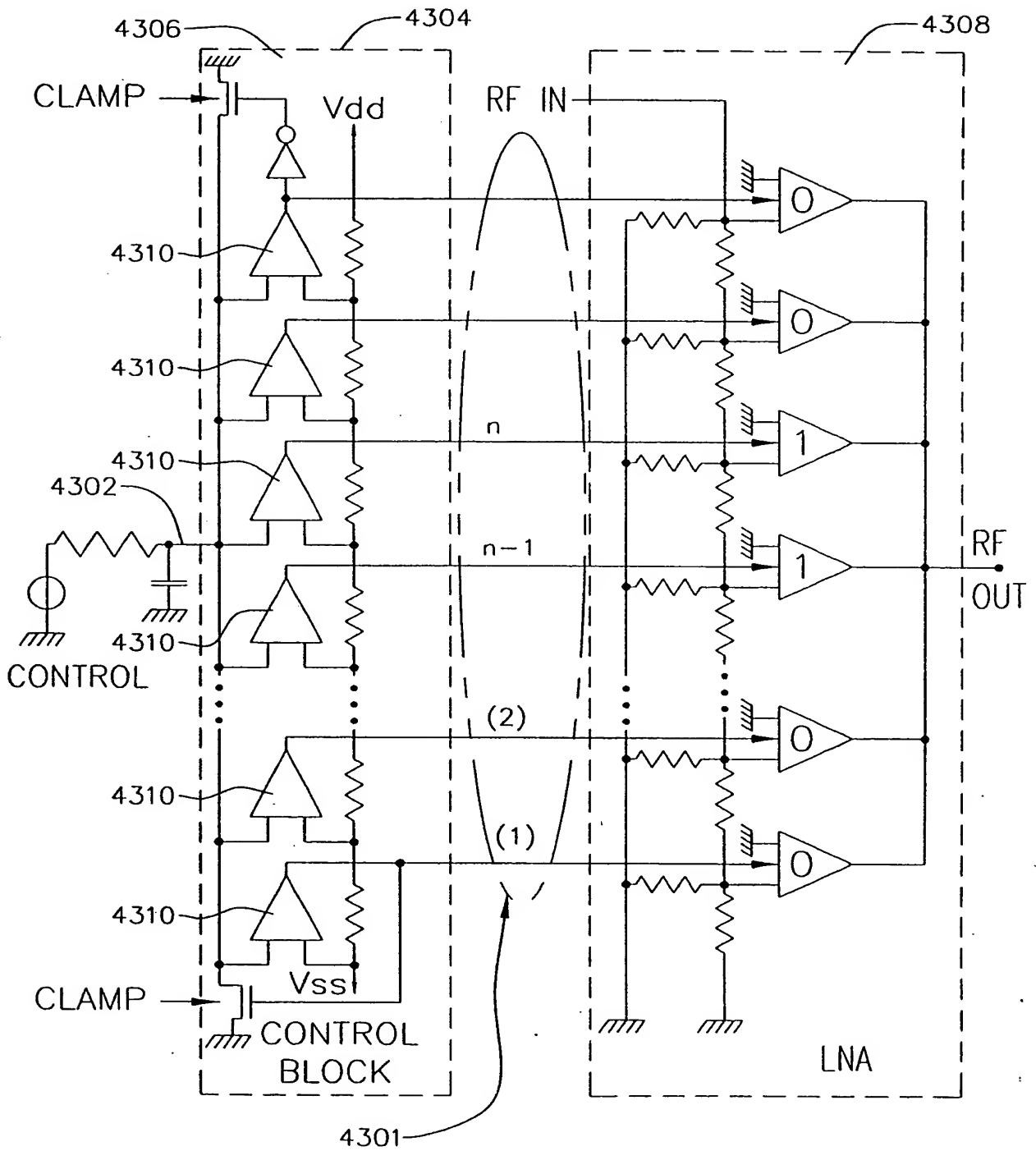


FIG. 42



**FIG. 43**

CLAMPING CONTROL RANGE.



**FIG. 44a**  
CONTROLLED GAIN COMPARATOR

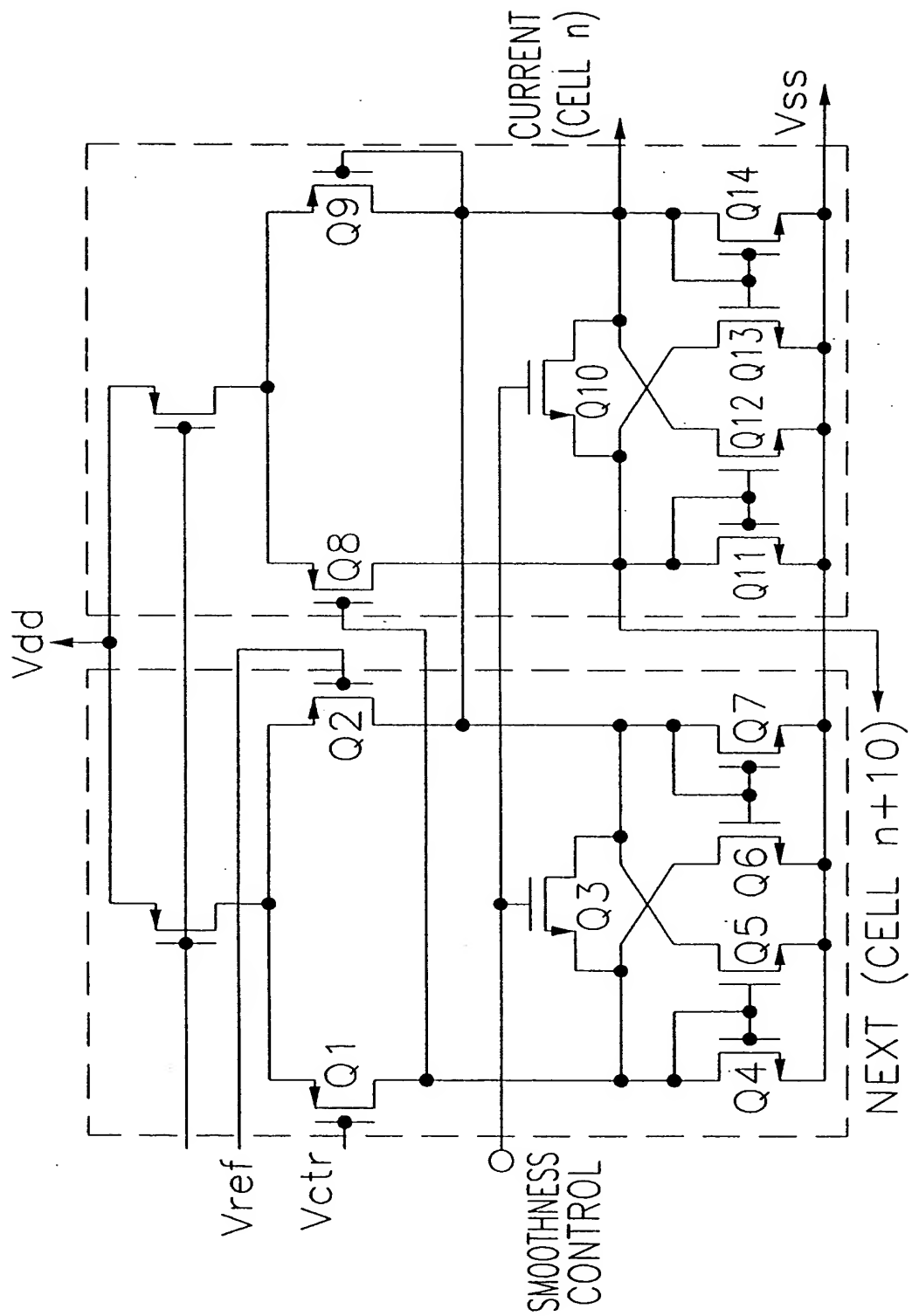




FIG. 45A

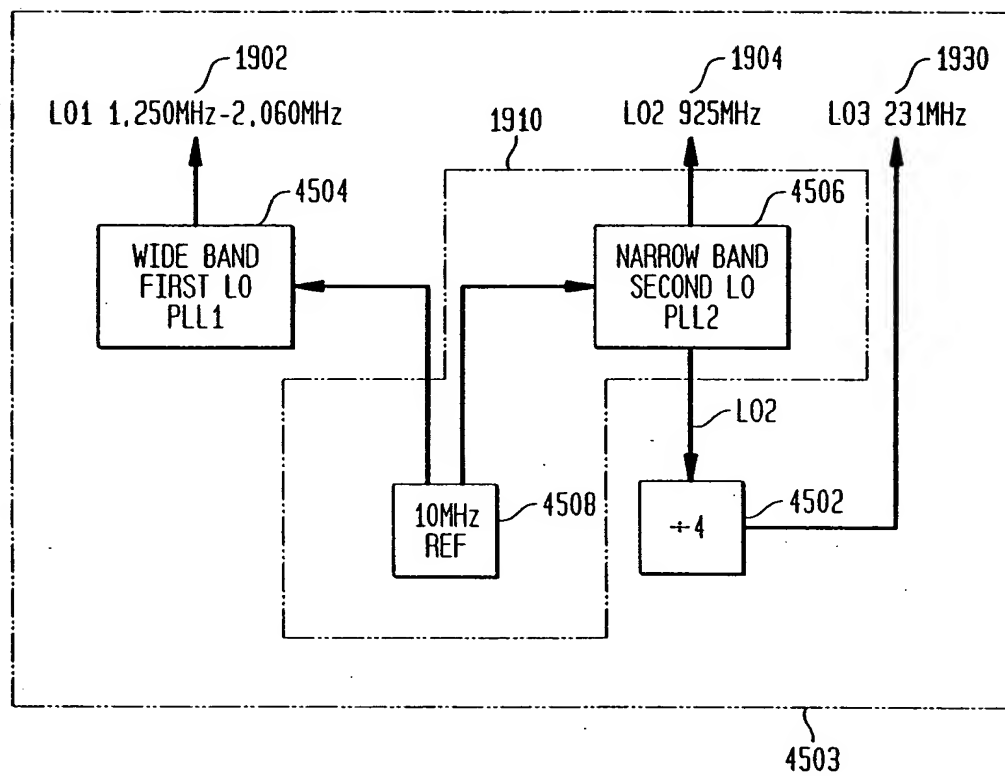


FIG. 45B

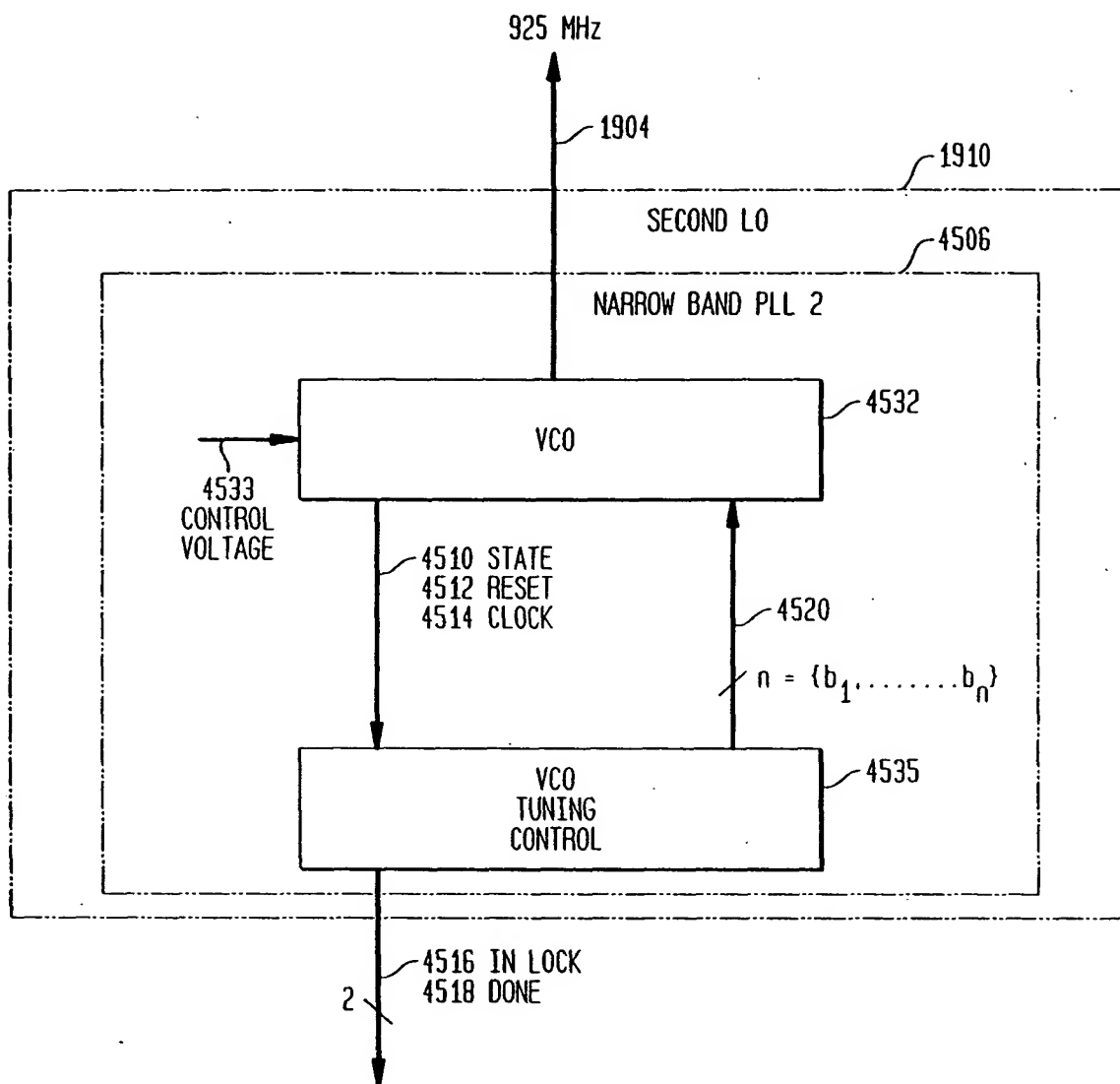


FIG. 45C

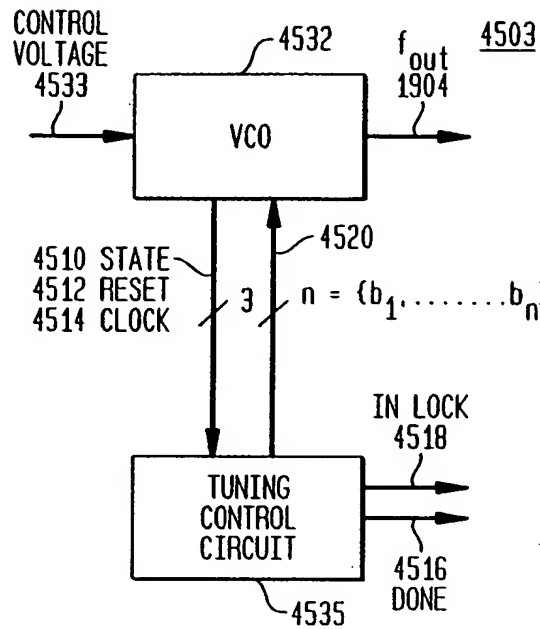


FIG. 45D

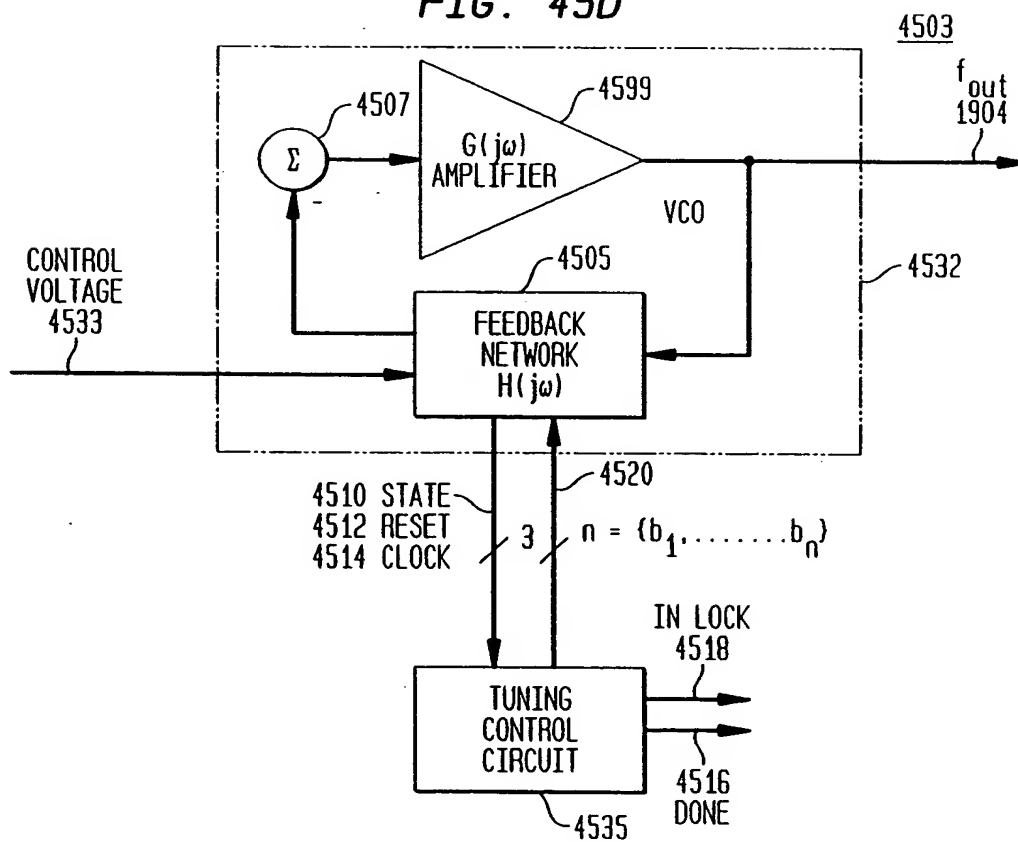


FIG. 45E

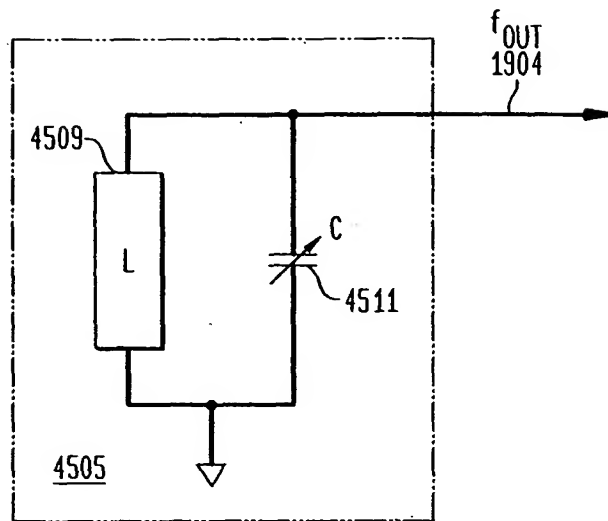
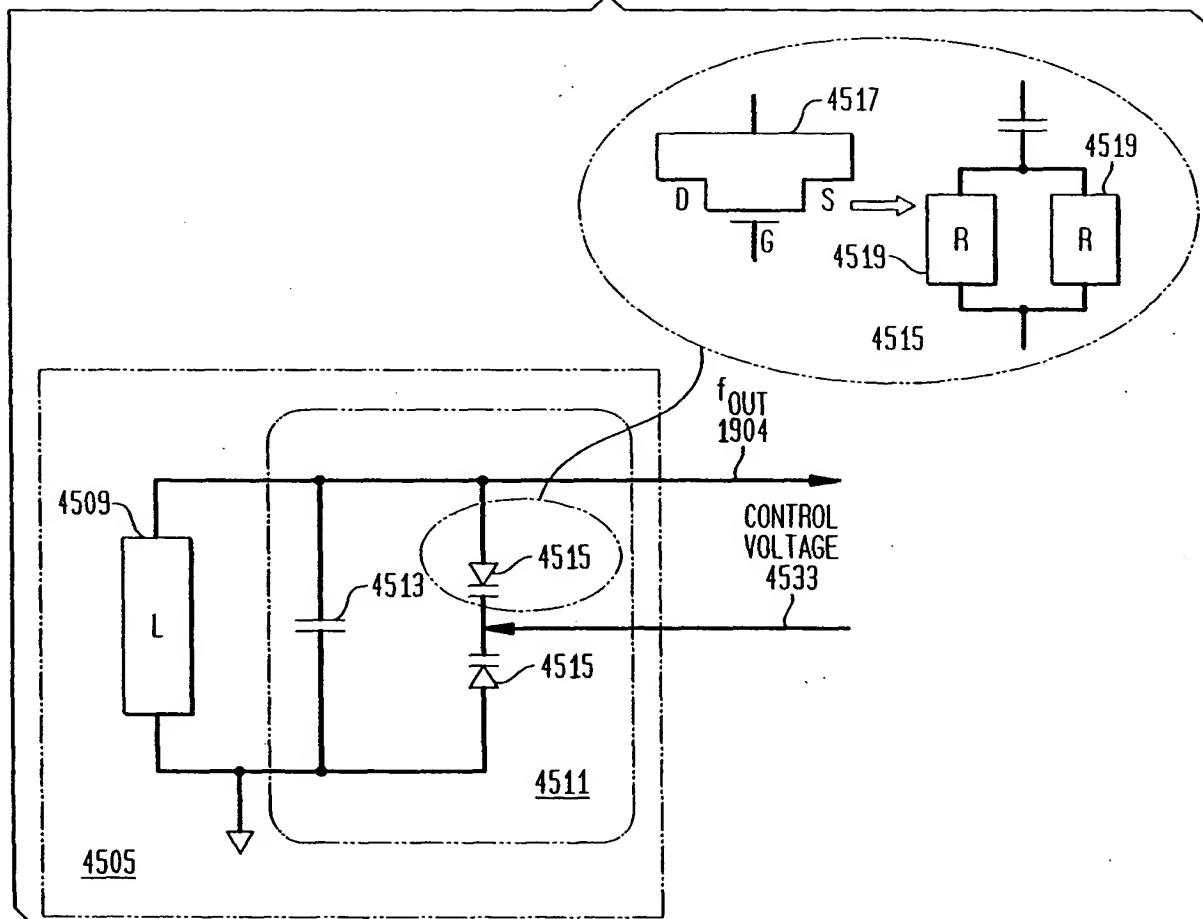
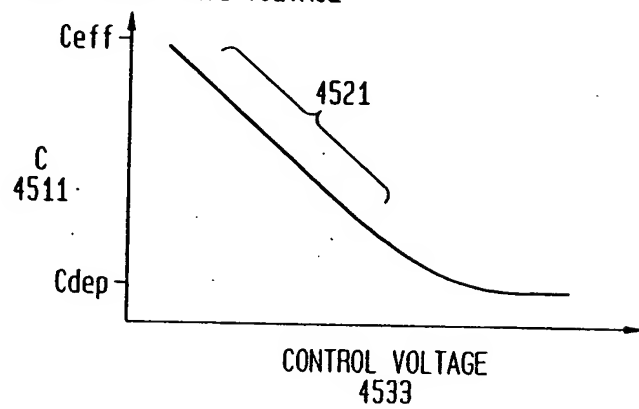


FIG. 45F

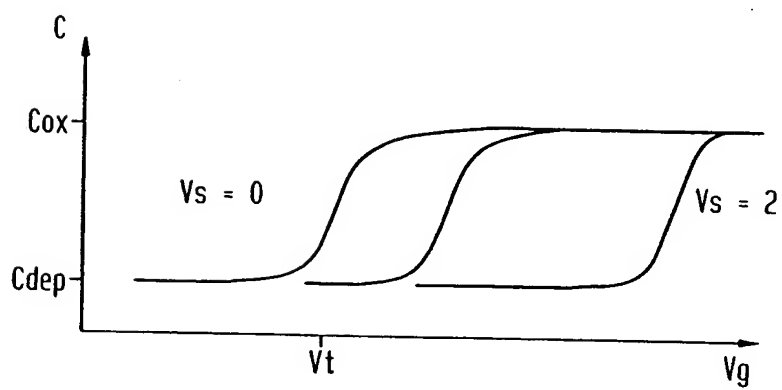


**FIG. 45G**

CAPACITANCE VS CONTROL VOLTAGE



**FIG. 45H**

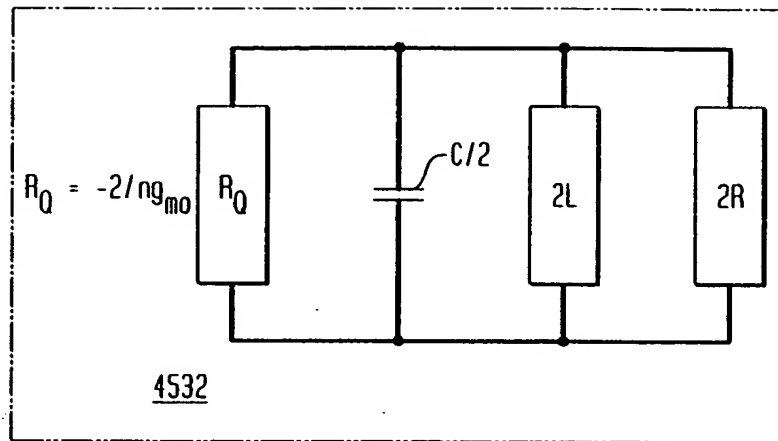


The diagram illustrates a multi-stage CMOS amplifier circuit, labeled 4532, which includes several key components and stages:

- Input Stage (4536):** A differential pair of NMOS transistors (M4, M6) with PMOS load devices (M5, M7). The PMOS devices are connected to  $V_{DD}$ . The NMOS devices have their sources connected to ground and their gates driven by a common-mode signal  $\Delta$ . Currents  $I$  are indicated through the PMOS devices.
- Adaptive Biasing (4530):** A feedback loop for biasing, consisting of a resistor (R, 4524, 100K) and a capacitor (4531, 1uF) connected to the gates of the input transistors. This is labeled "ADAPTIVE BIAS".
- NMOS Drivers (4528):** A series of NMOS transistors (4527) connected in a chain. The gates of these transistors are driven by a common-mode signal  $\Delta$ . The sources are connected to ground, and the drains are connected to the gates of the input transistors (M4, M6). This stage is labeled "NMOS DRIVERS".
- Control Voltage (4509):** A control voltage source (4509) connected to the gates of the NMOS drivers (4527) and the input transistors (M4, M6). This is labeled "CONTROL VOLTAGE".
- Output Stage (4539):** A differential pair of NMOS transistors (M1, M2) with PMOS load devices (4520). The PMOS devices are connected to  $V_{DD}$ . The NMOS devices have their sources connected to ground and their gates driven by a common-mode signal  $\Delta$ . The output of the amplifier is taken from the drains of the NMOS devices (M1, M2) and is labeled  $f_{OUT}$  1904.
- Other Components:** The circuit includes various capacitors (4526, 4527, 4528, 4529, 4530, 4531, 4532) and resistors (4524, 4525, 4526, 4527, 4528, 4529, 4530, 4531, 4532) connected to the gates and drains of the transistors.

$$\begin{array}{r} 4507 \\ \underline{4505} \end{array}$$

**FIG. 45J**



**FIG. 45K**

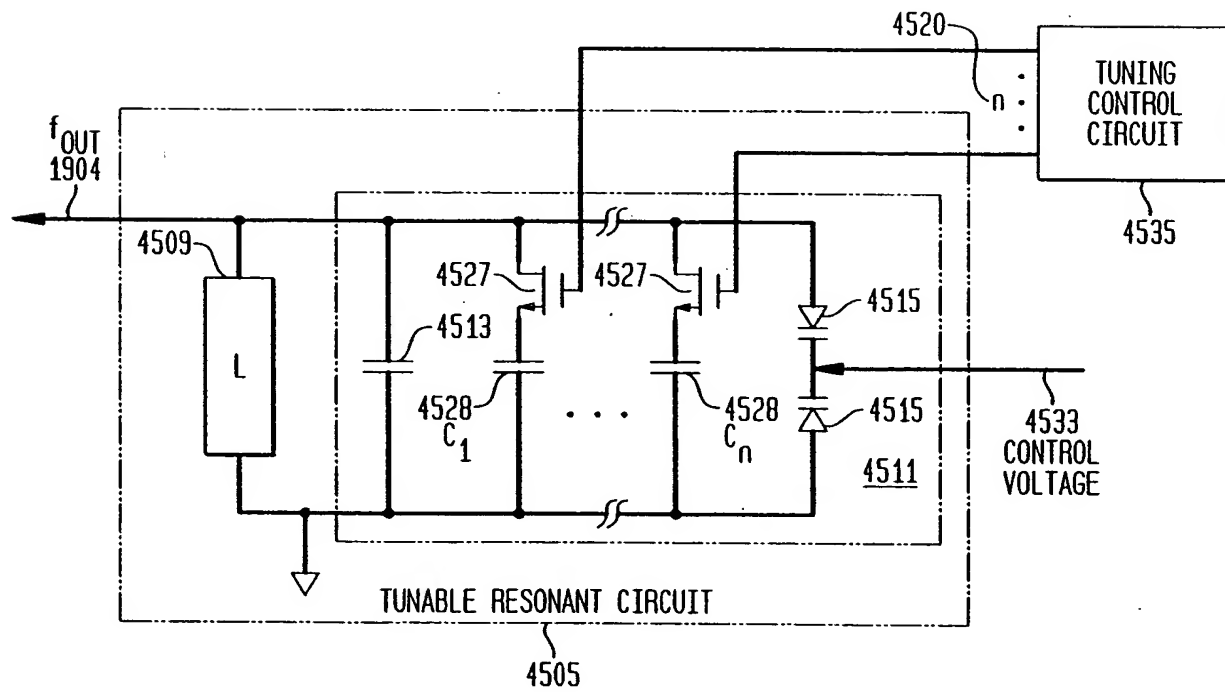


FIG. 46A

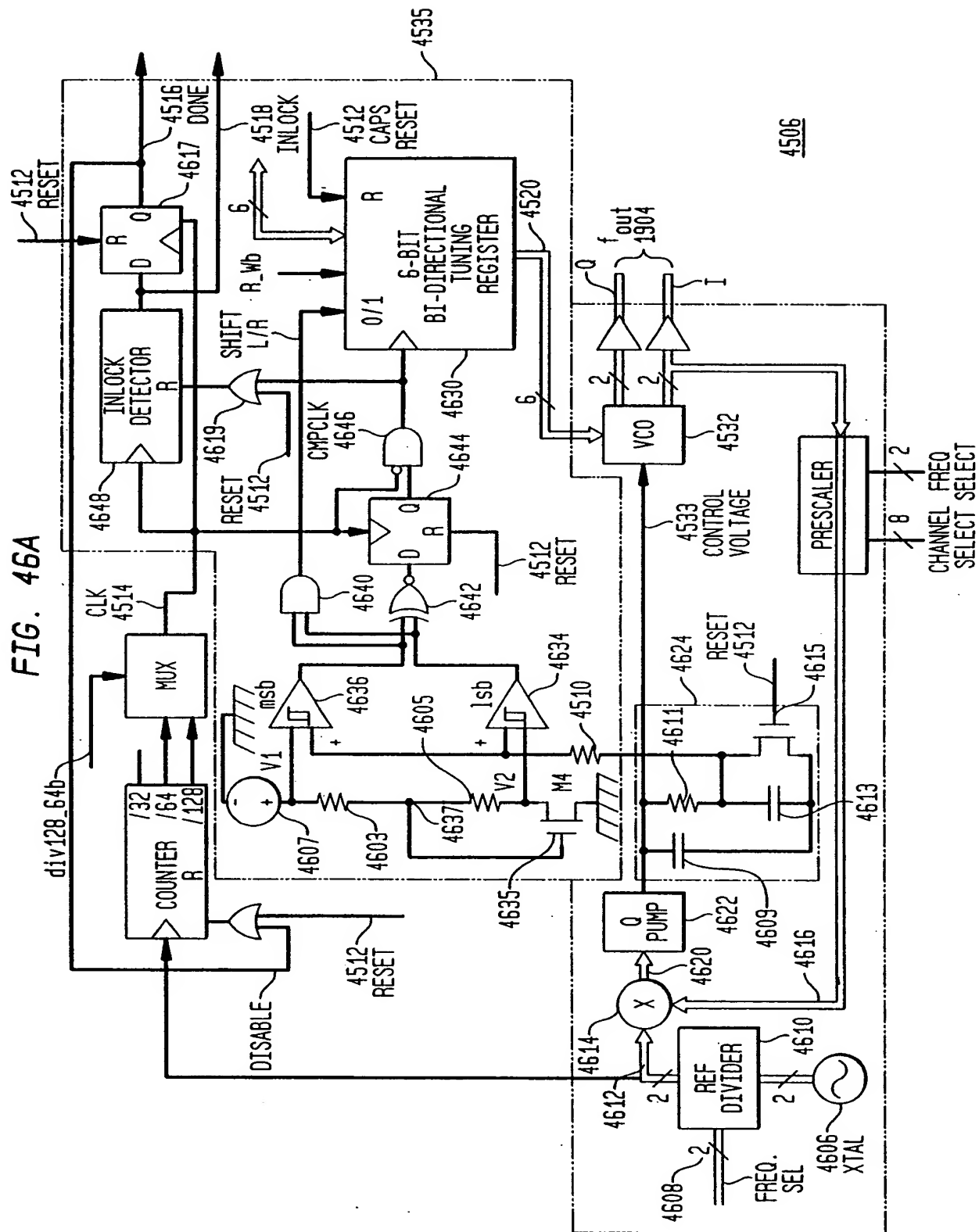


FIG. 46B

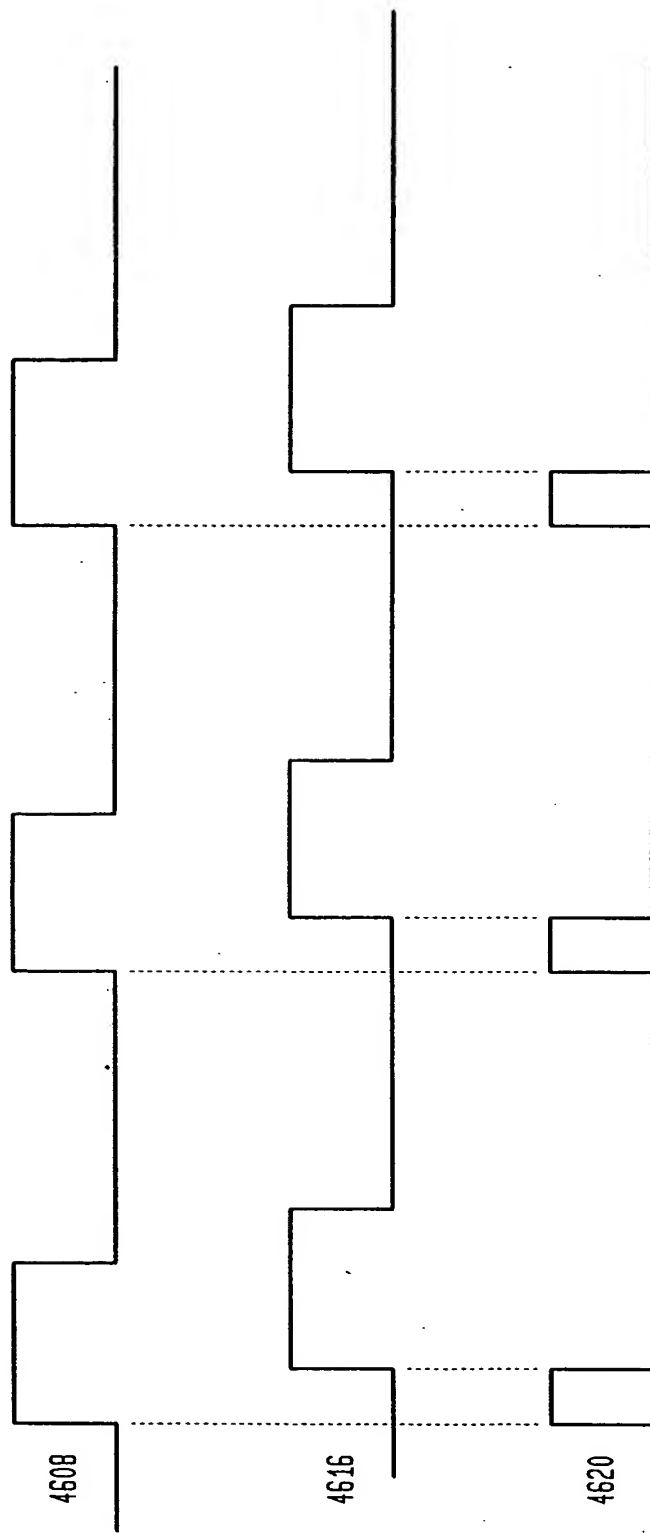


FIG. 47A

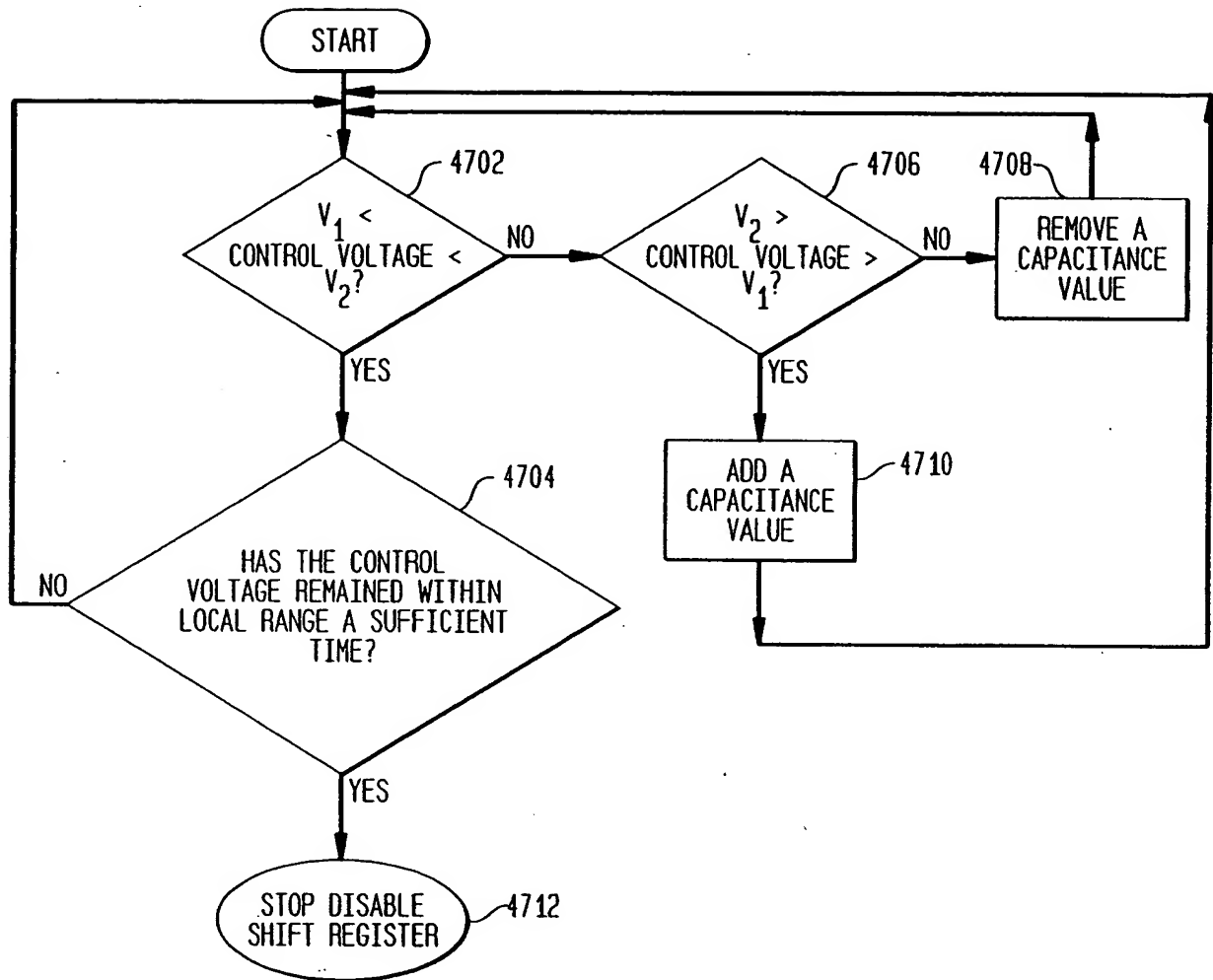


FIG. 47B

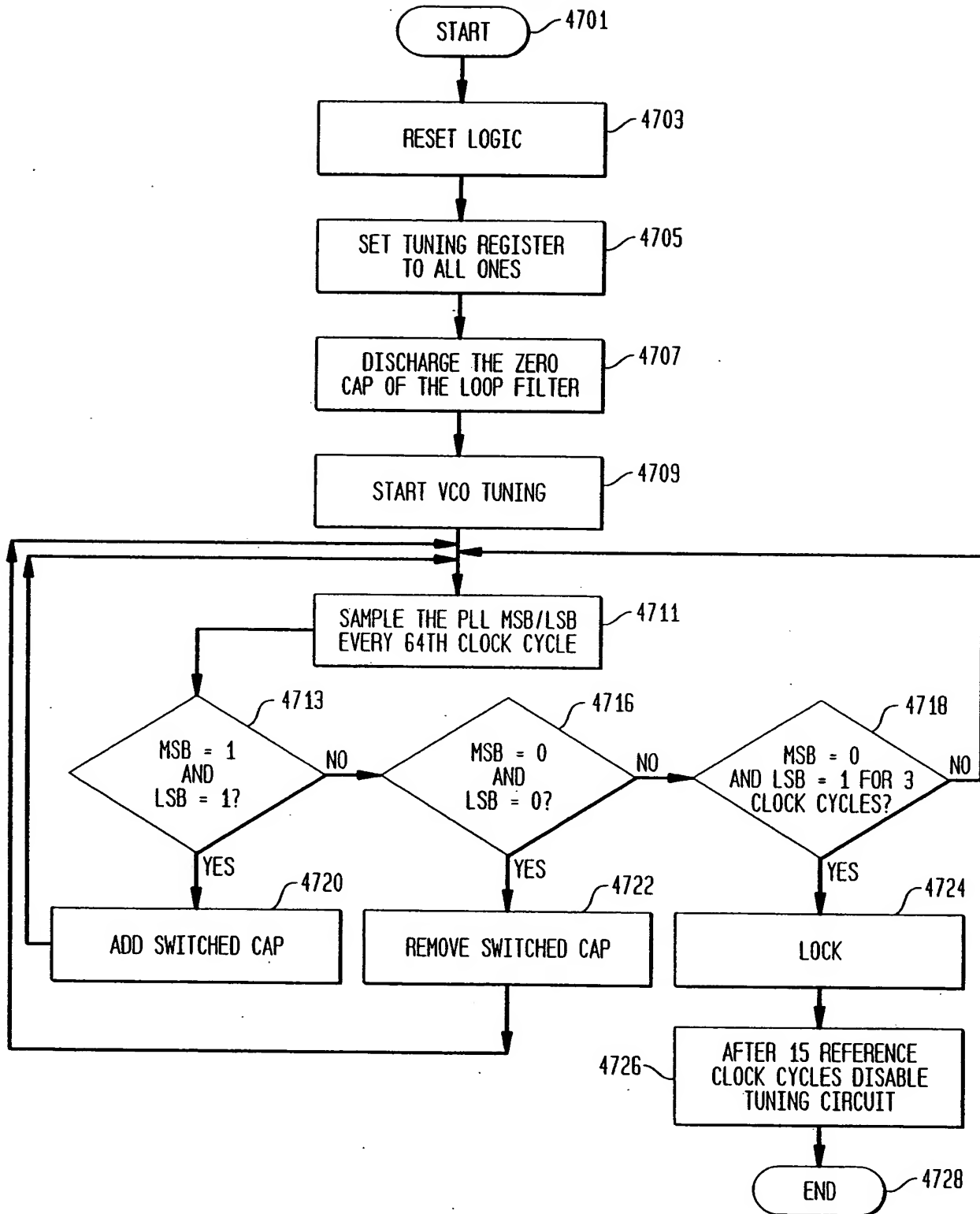


FIG. 47C

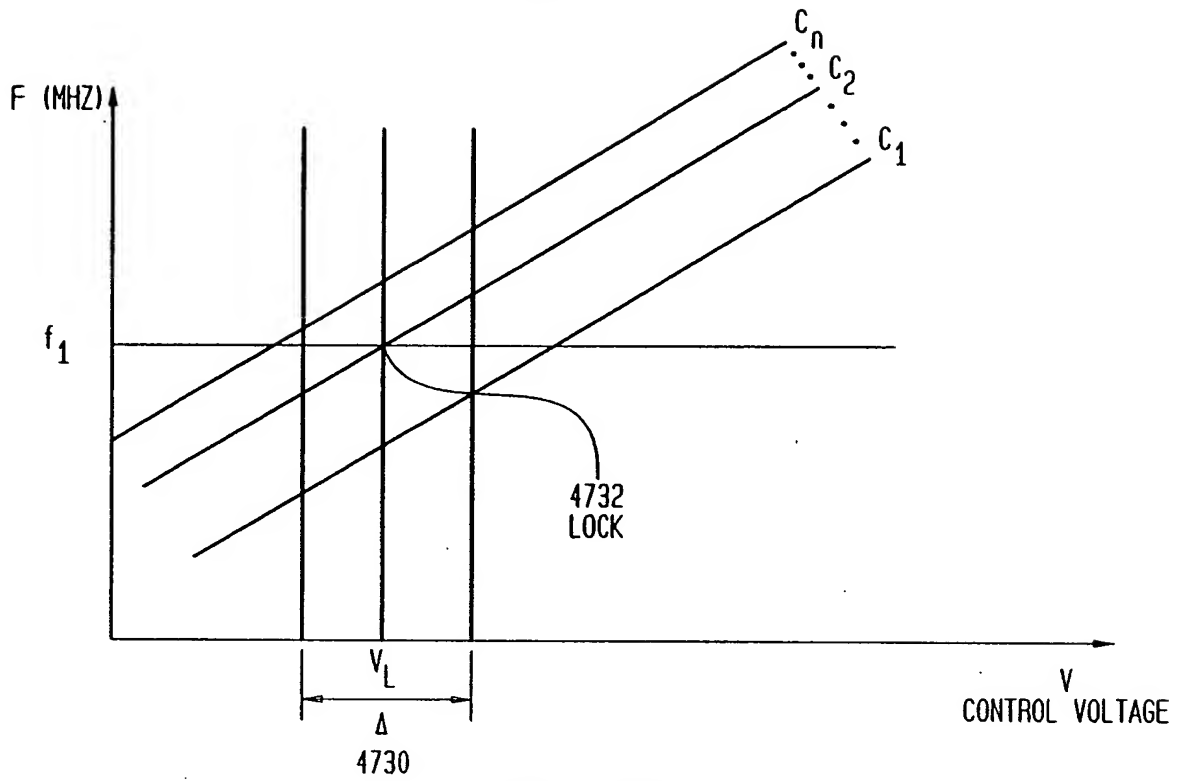
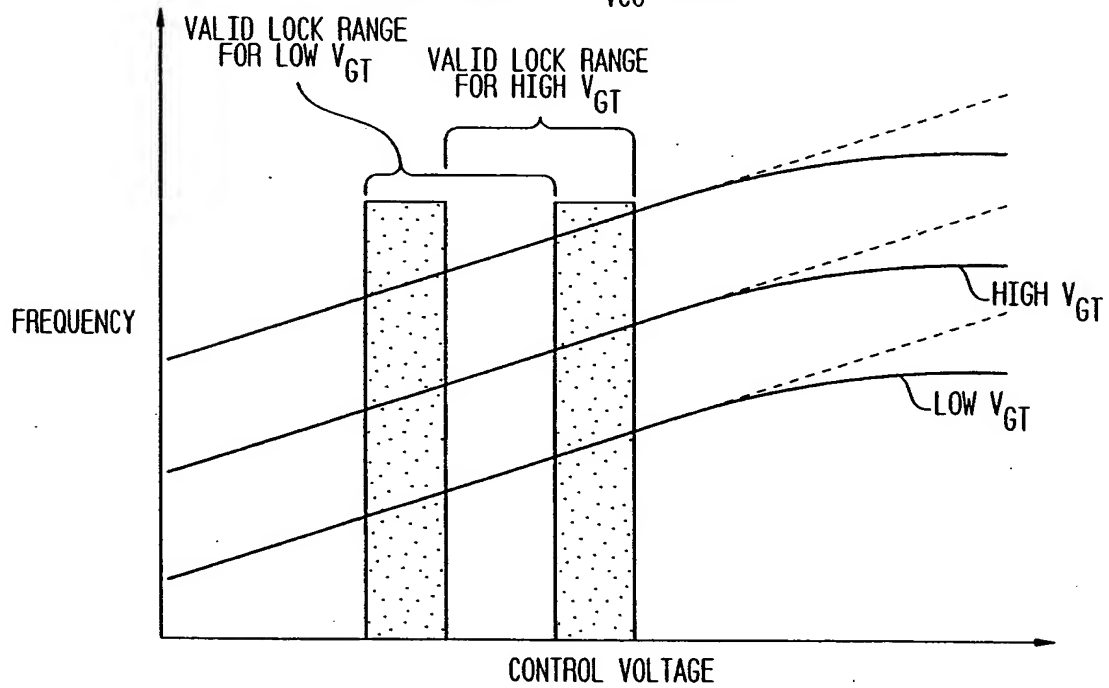


FIG. 47D

REPRESENTATIVE  $K_{VCO}$  CURVES



EXTERNAL 36 OR 44MHz FILTER OPTION  
E.G.SIEMENS X6964( $f_c=43.75\text{MHz}$ )

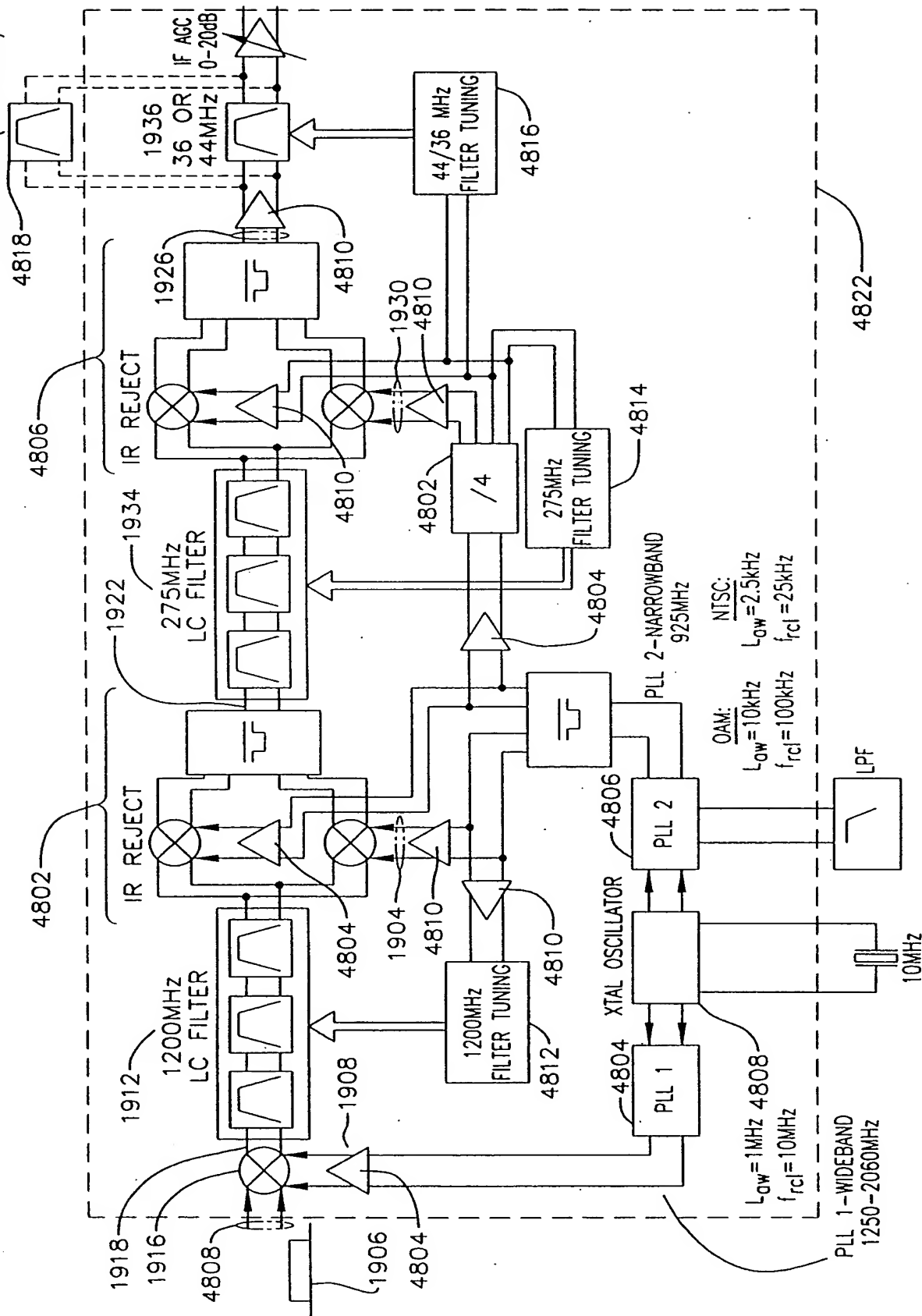


FIG. 49

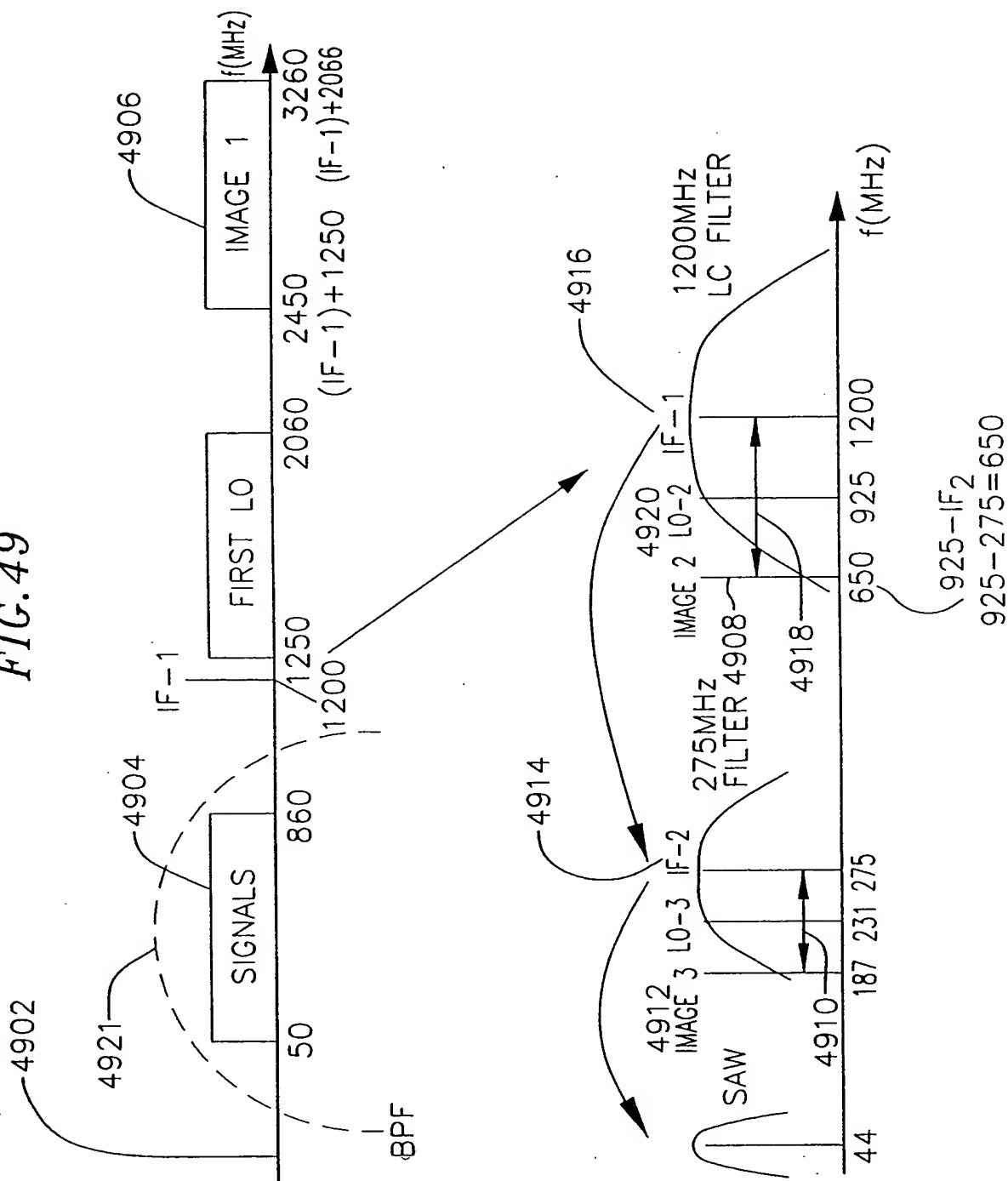
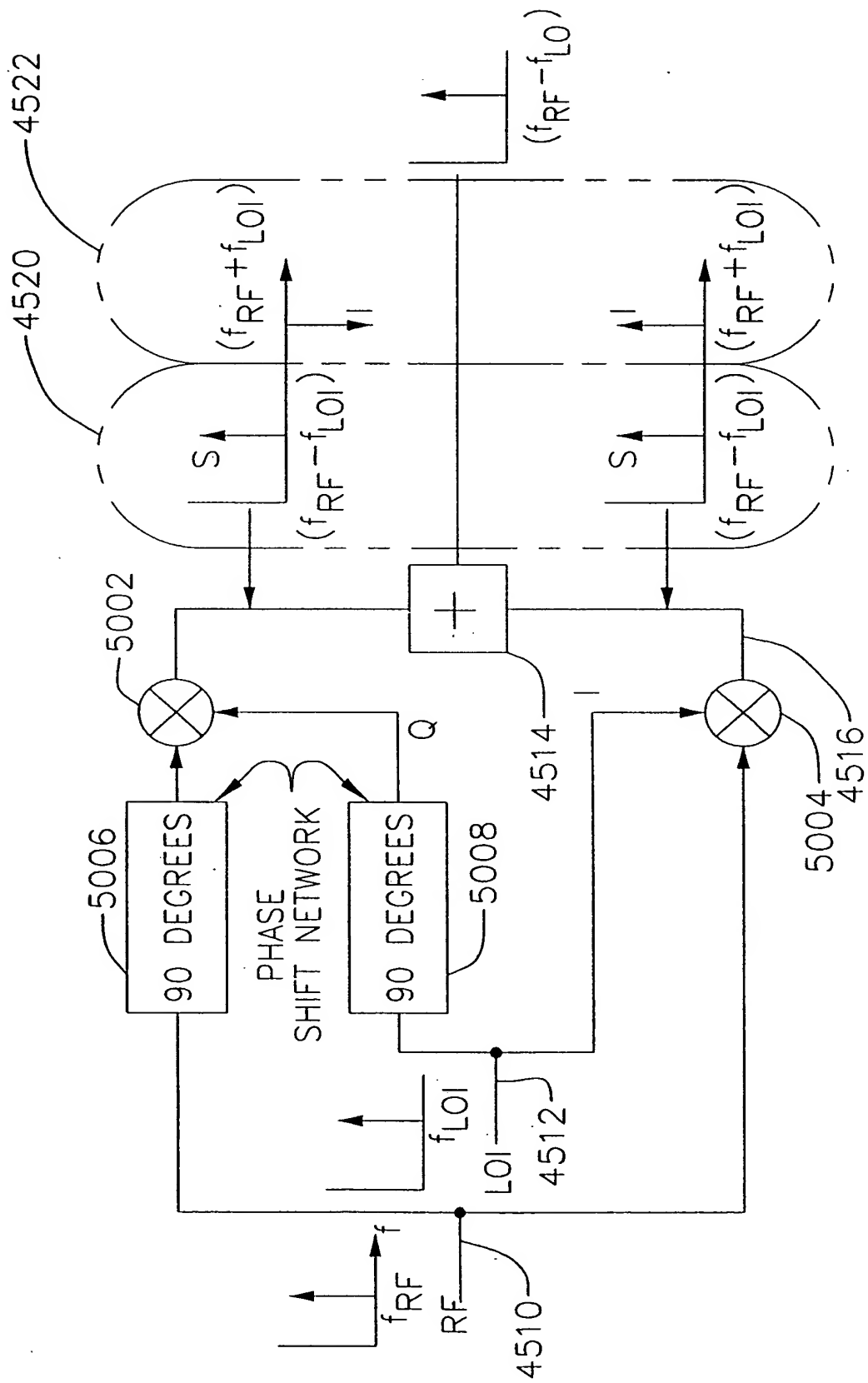
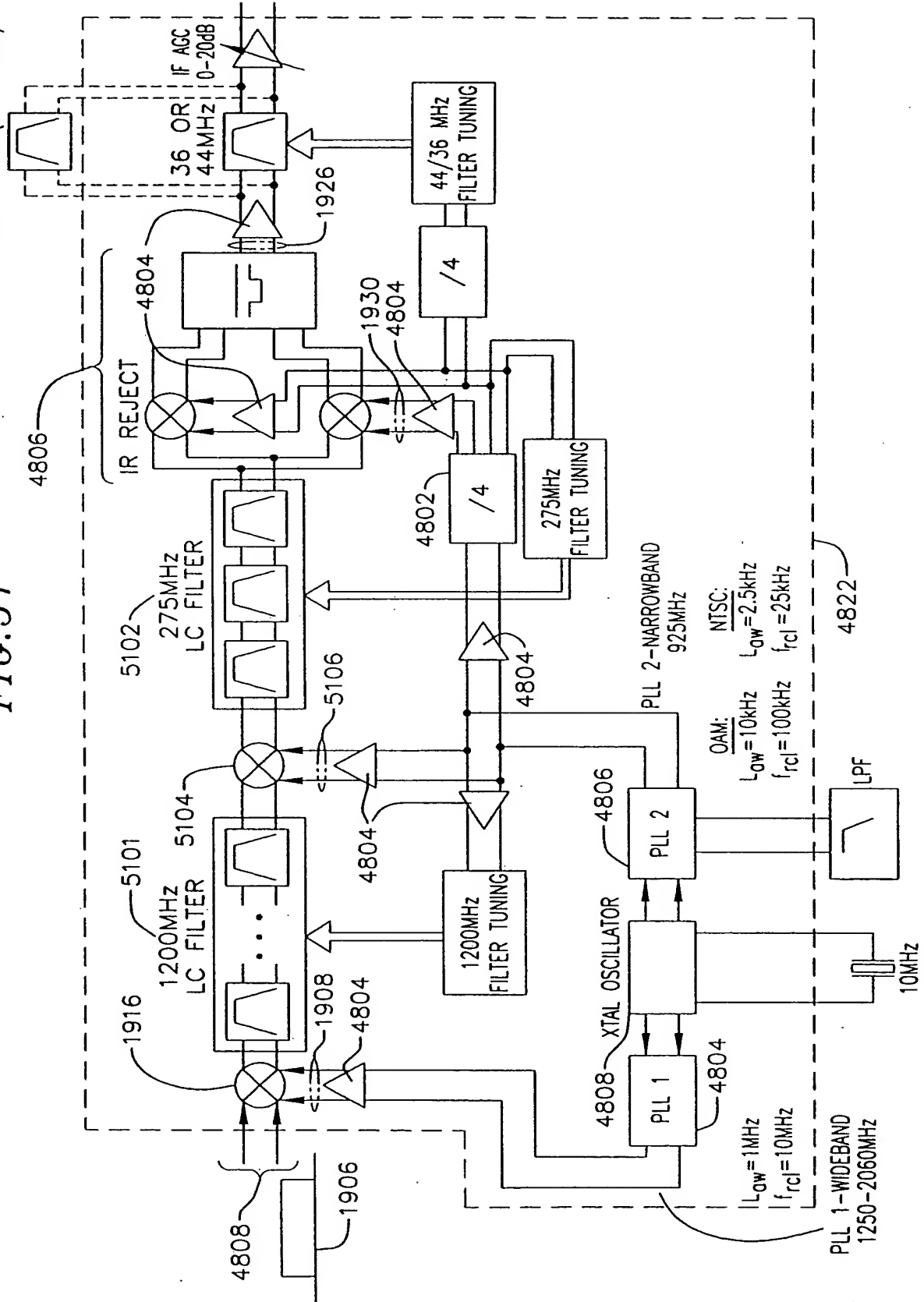


FIG. 50



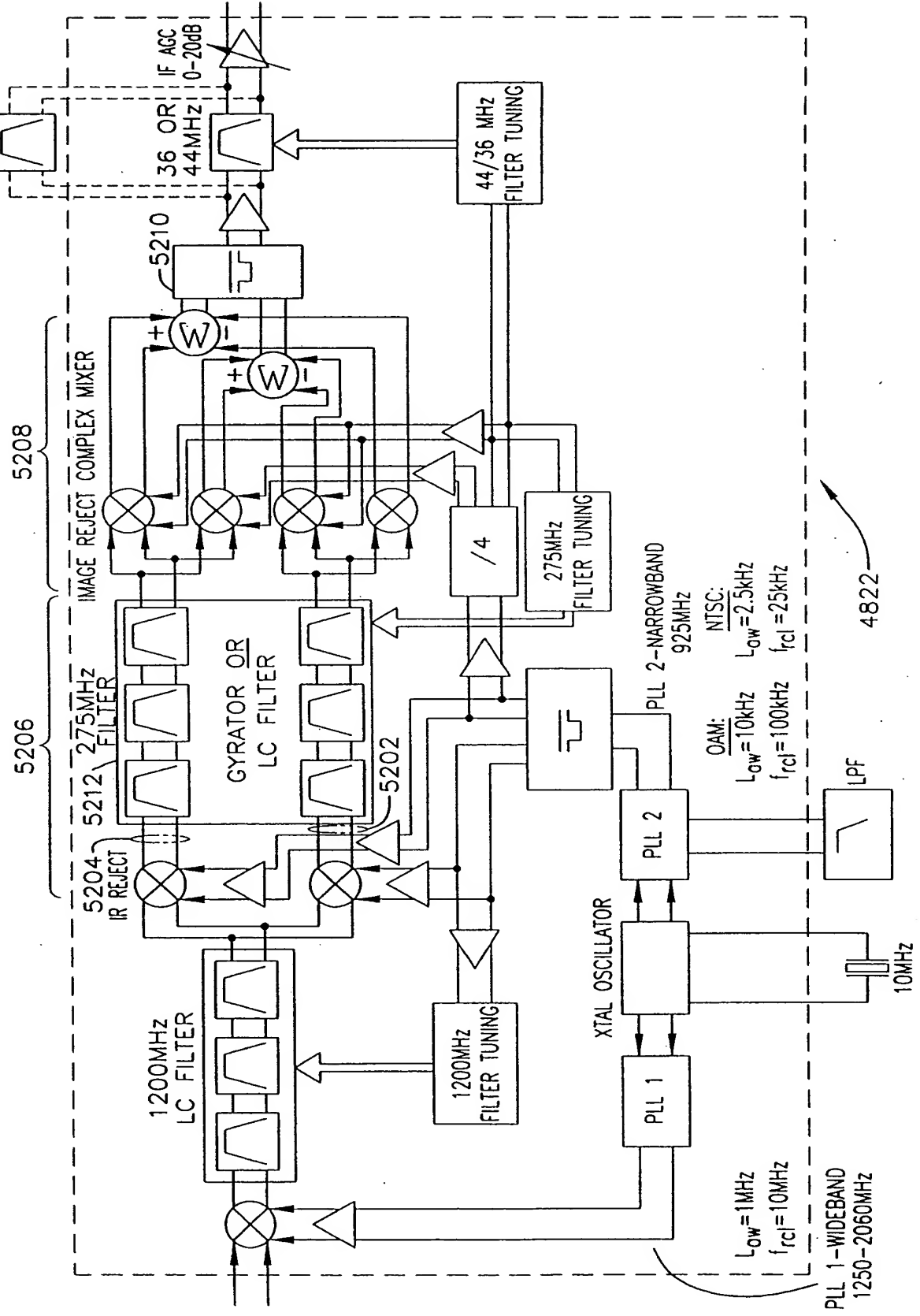
EXTERNAL 36 OR 44MHz FILTER OPTION  
E.G. SIEMENS X6964 ( $f_c=43.75\text{MHz}$ )

FIG. 51



EXTERNAL 36 OR 44MHz FILTER OPTION  
E.G. SIEMENS X6964 ( $f_c = 43.75\text{MHz}$ )

FIG. 52



# FIG.53

CATV TUNER

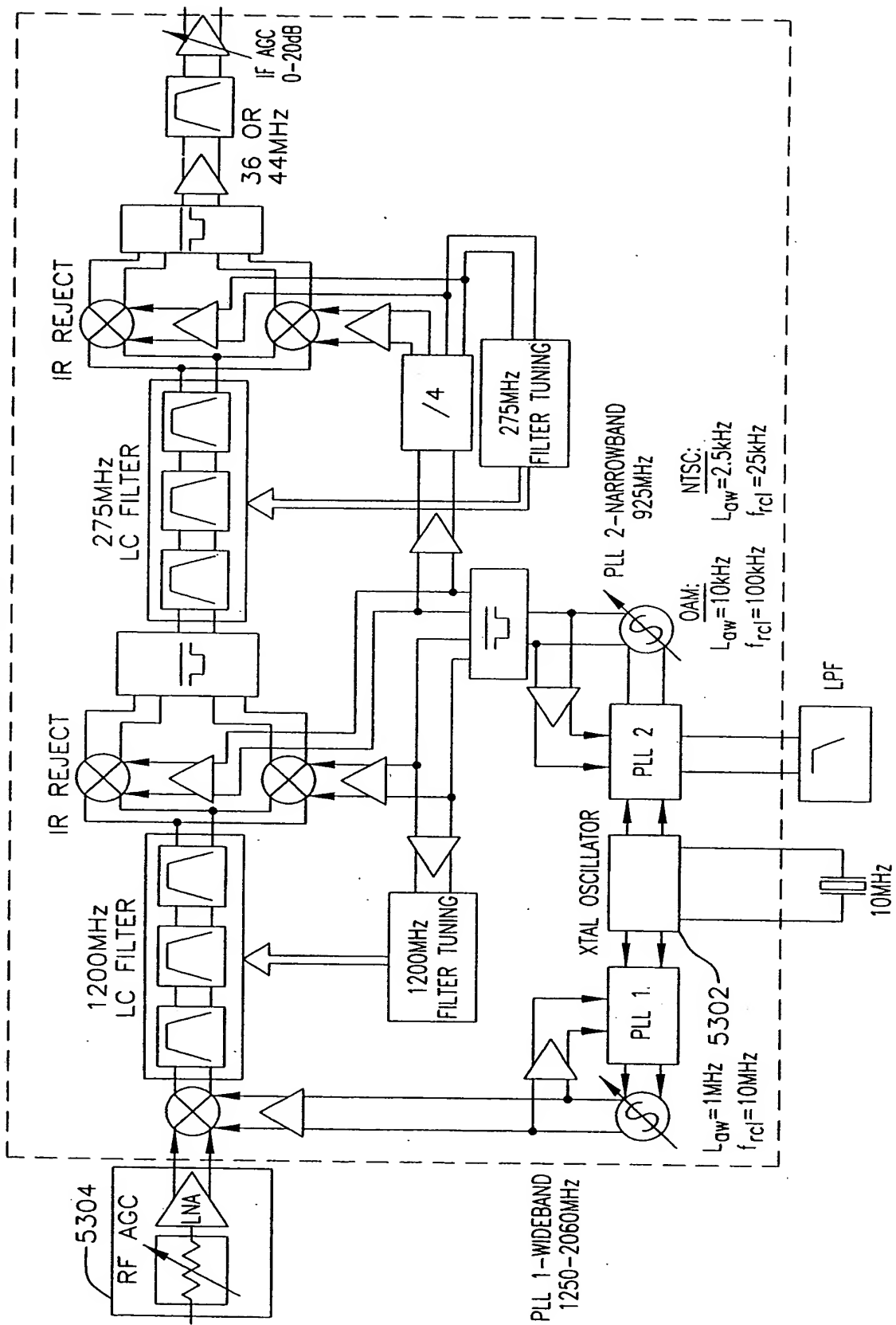
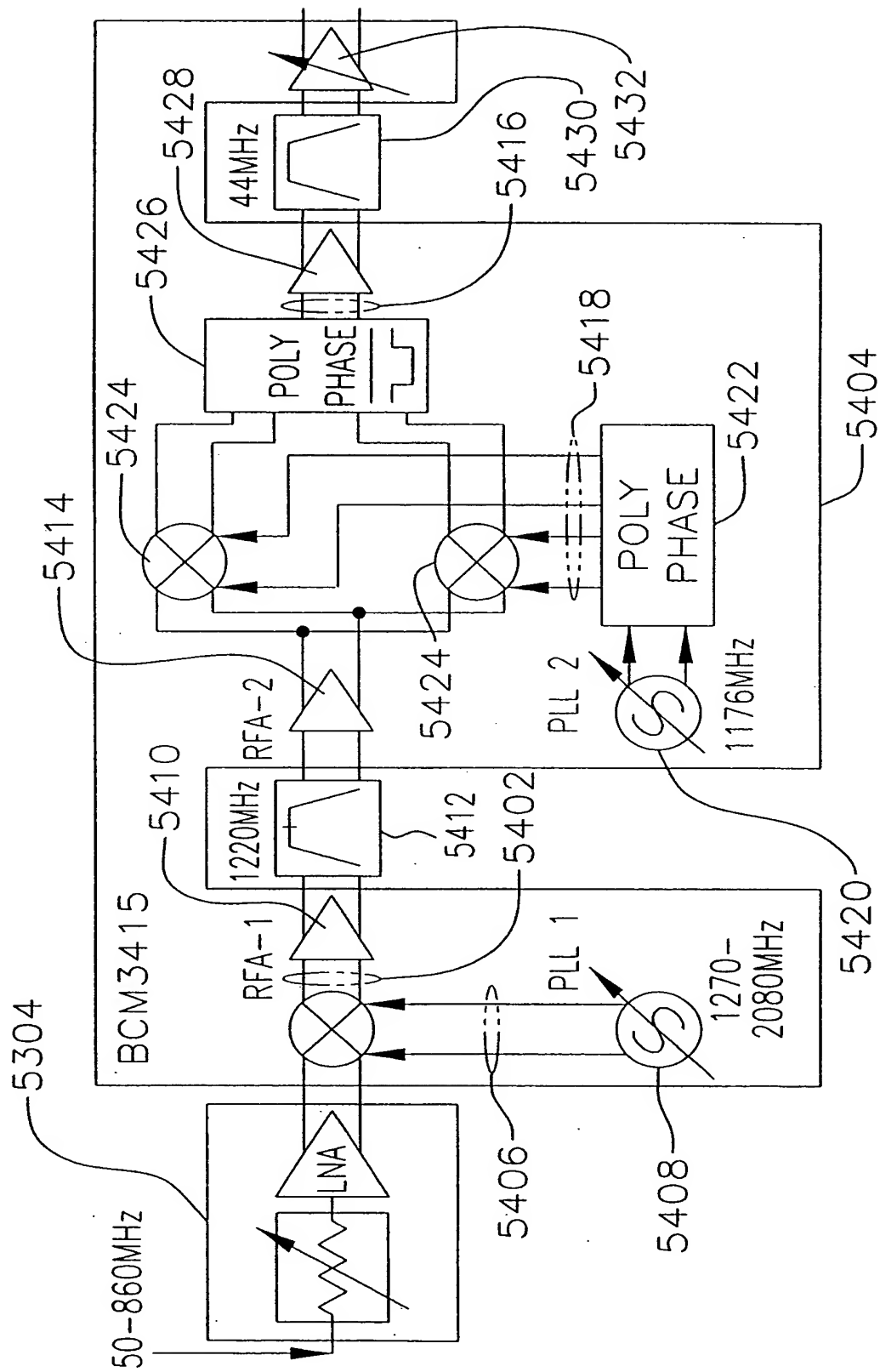
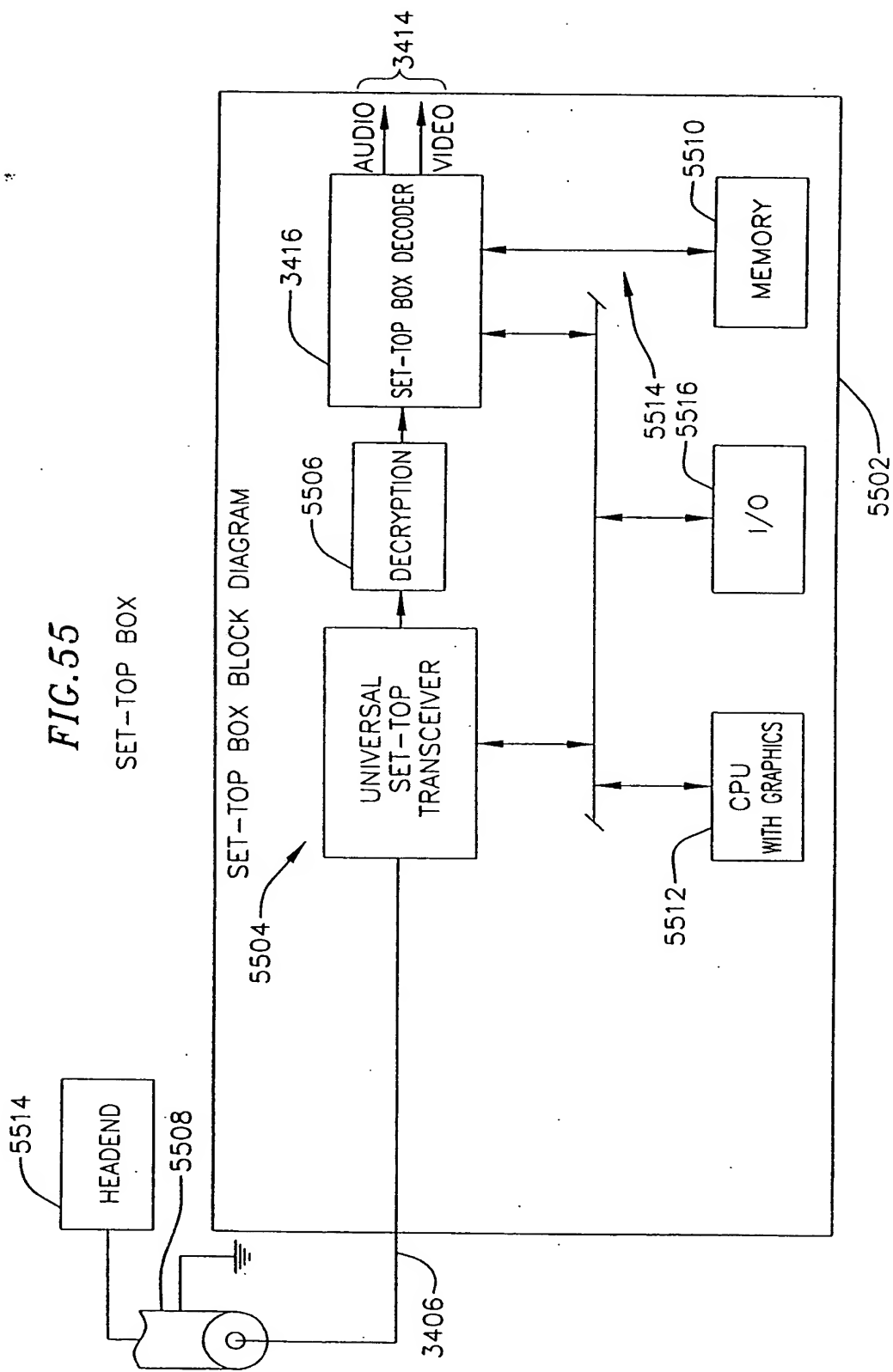


FIG. 54





**FIG. 56**  
TELEVISION

The diagram illustrates a television receiver system, labeled FIG. 56. The system is divided into several functional blocks, some of which are grouped within dashed-line enclosures.

**Input and Tuning Section:** The system receives signals from an antenna (labeled "V OR") or a cable (labeled "OR"). These signals pass through a "TUNER" (3408) and a "PROG. ATTEN/LNA" (variable attenuator/low noise amplifier) block. The output of the tuner is fed into a "VIF AMPLIFIER" (5620).

**Intermediate Frequency (IF) and Video Processing Section:** The "VIF AMPLIFIER" (5620) is controlled by an "RF AGC" (5604). Its output goes to a "VIDEO DETECTOR" (5622), which is controlled by an "IF AGC" (5604). The "VIDEO DETECTOR" (5622) outputs to a "VIDEO PROCESS" block (5610), which is controlled by a "VIDEO PROCESS" block (5604). The "VIDEO PROCESS" (5610) also receives feedback from an "FM DETECTOR" (5610) and an "AUDIO OUT" block (5608).

**Audio and Video Output Section:** The "VIDEO PROCESS" (5610) outputs to a "VIDEO OUT" block (5606), which is controlled by a "VIDEO PROCESS" block (5604). The "VIDEO OUT" (5606) outputs to an "AUDIO OUT" block (5608), which is controlled by an "FM DETECTOR" (5610). The "AUDIO OUT" (5608) is connected to a speaker (5602). The "VIDEO OUT" (5606) also outputs to a "CHROMA DEMODULATOR" (5604), which is controlled by a "CHROMA SYNC" block (5604).

**Color and Sync Processing Section:** The "CHROMA DEMODULATOR" (5604) outputs to a "CHROMA SYNC" block (5604), which is controlled by a "CHROMA SYNC" block (5604). The "CHROMA SYNC" (5604) outputs to a "HORIZONTAL PROCESS" block (5612) and a "VERTICAL PROCESS" block (5612). The "HORIZONTAL PROCESS" (5612) outputs to a "HORIZONTAL DRIVE" block (5612), which is controlled by a "HORIZONTAL PROCESS" block (5612). The "VERTICAL PROCESS" (5612) outputs to a "VERTICAL DRIVE" block (5612), which is controlled by a "VERTICAL PROCESS" block (5612).

**Output Section:** The "HORIZONTAL DRIVE" (5612) outputs to a "HORIZONTAL OUT" block (5614), which is controlled by a "HORIZONTAL OUT" block (5614). The "VERTICAL DRIVE" (5612) outputs to a "VERTICAL OUT" block (5614), which is controlled by a "VERTICAL OUT" block (5614). The "HORIZONTAL OUT" (5614) and "VERTICAL OUT" (5614) blocks are connected to a speaker (5602).

**Control and Monitoring Section:** A "NOISE CANCEL" block (5604) is connected to the "HORIZONTAL PROCESS" (5612) and "VERTICAL PROCESS" (5612) blocks. A "SYNC SEPARATOR" block (5604) is connected to the "HORIZONTAL PROCESS" (5612) and "VERTICAL PROCESS" (5612) blocks. A "CHROMA SYNC" block (5604) is connected to the "CHROMA DEMODULATOR" (5604) and "HORIZONTAL PROCESS" (5612) blocks. A "VIDEO PROCESS" block (5604) is connected to the "VIDEO DETECTOR" (5622) and "VIDEO PROCESS" (5610) blocks. An "FM DETECTOR" block (5610) is connected to the "VIDEO DETECTOR" (5622) and "AUDIO OUT" (5608) blocks. An "IF AGC" block (5604) is connected to the "VIDEO DETECTOR" (5622) and "IF AGC" (5604) blocks. An "RF AGC" block (5604) is connected to the "VIF AMPLIFIER" (5620) and "RF AGC" (5604) blocks.

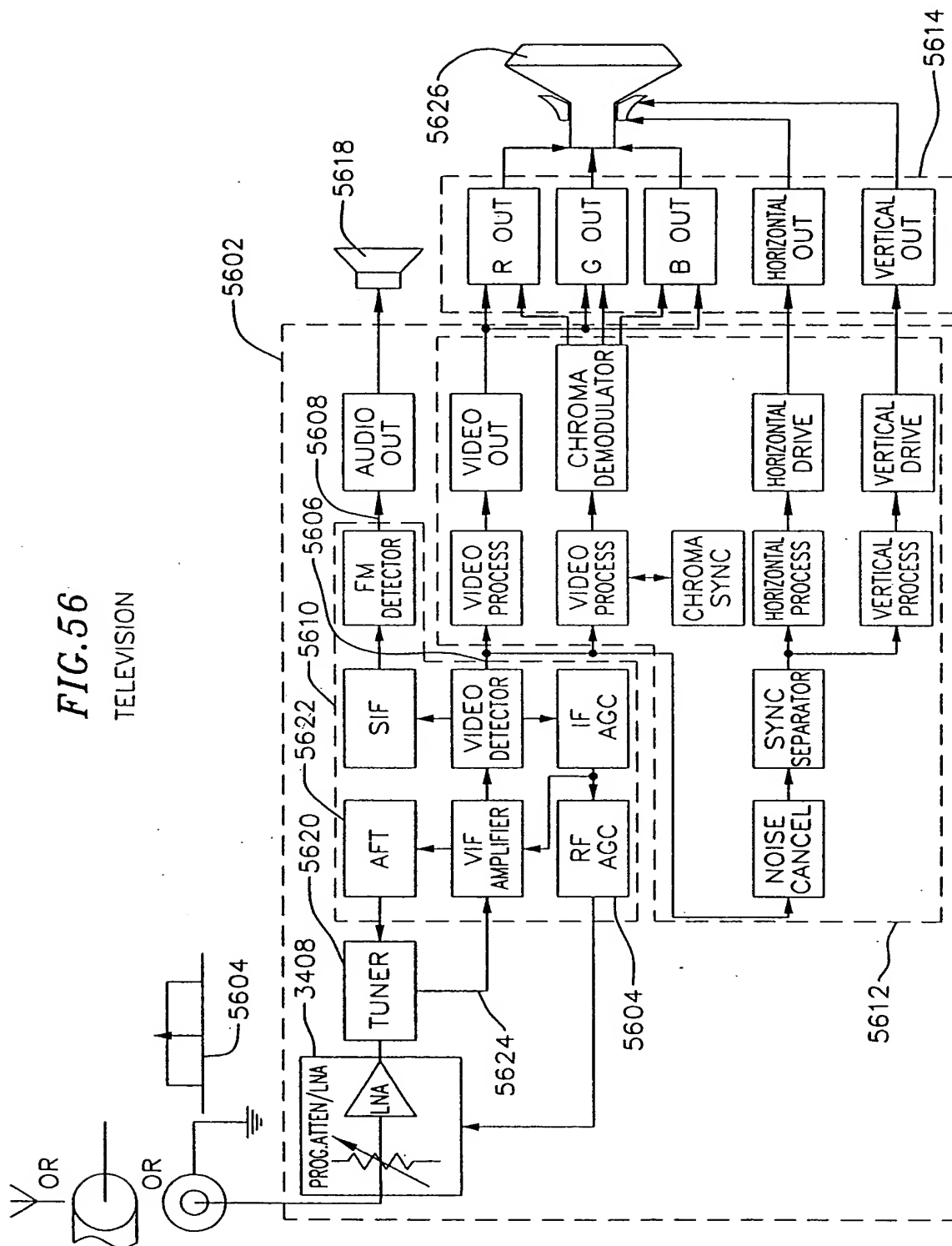


FIG. 57

VCR BLOCK DIAGRAM

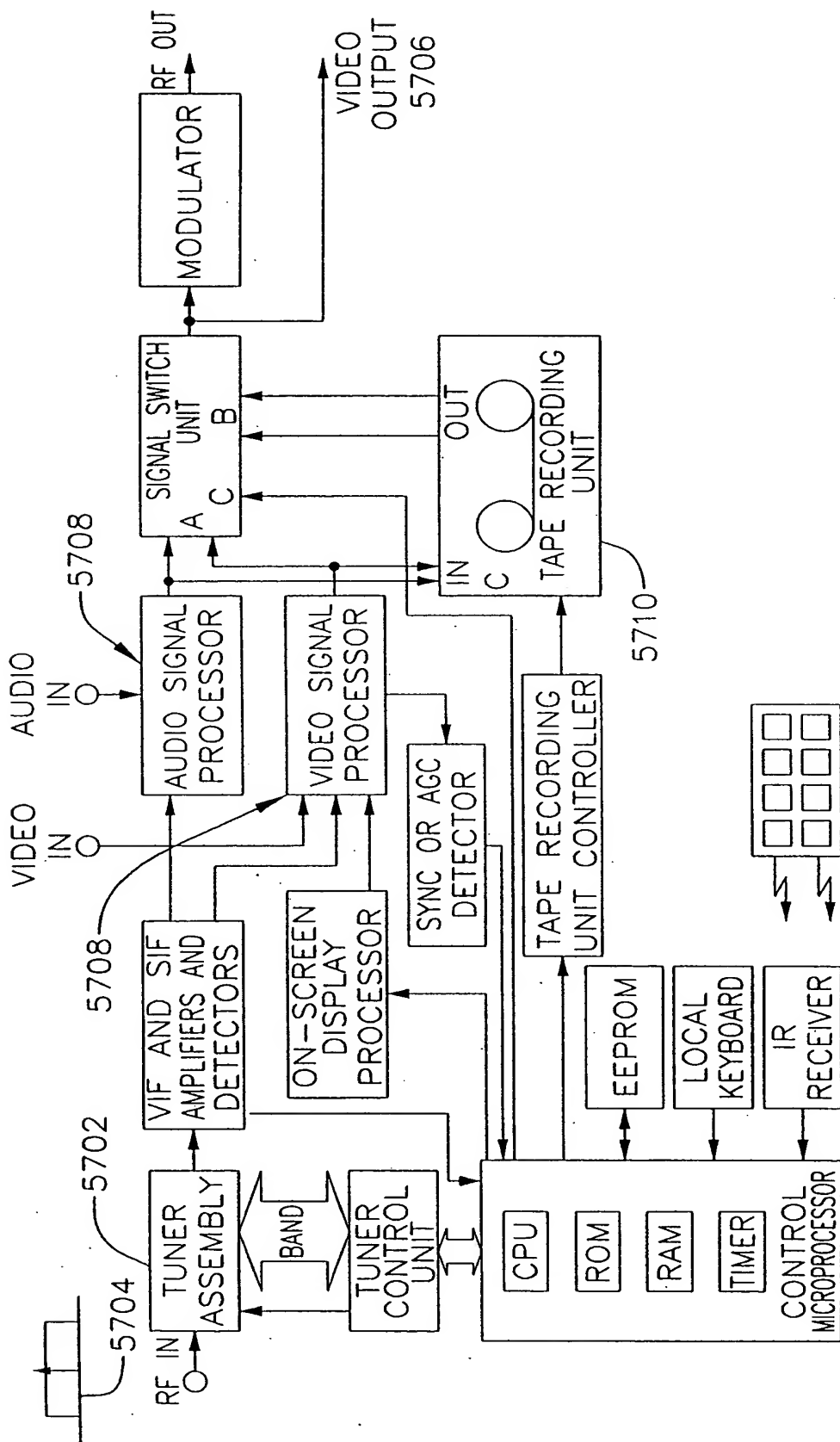
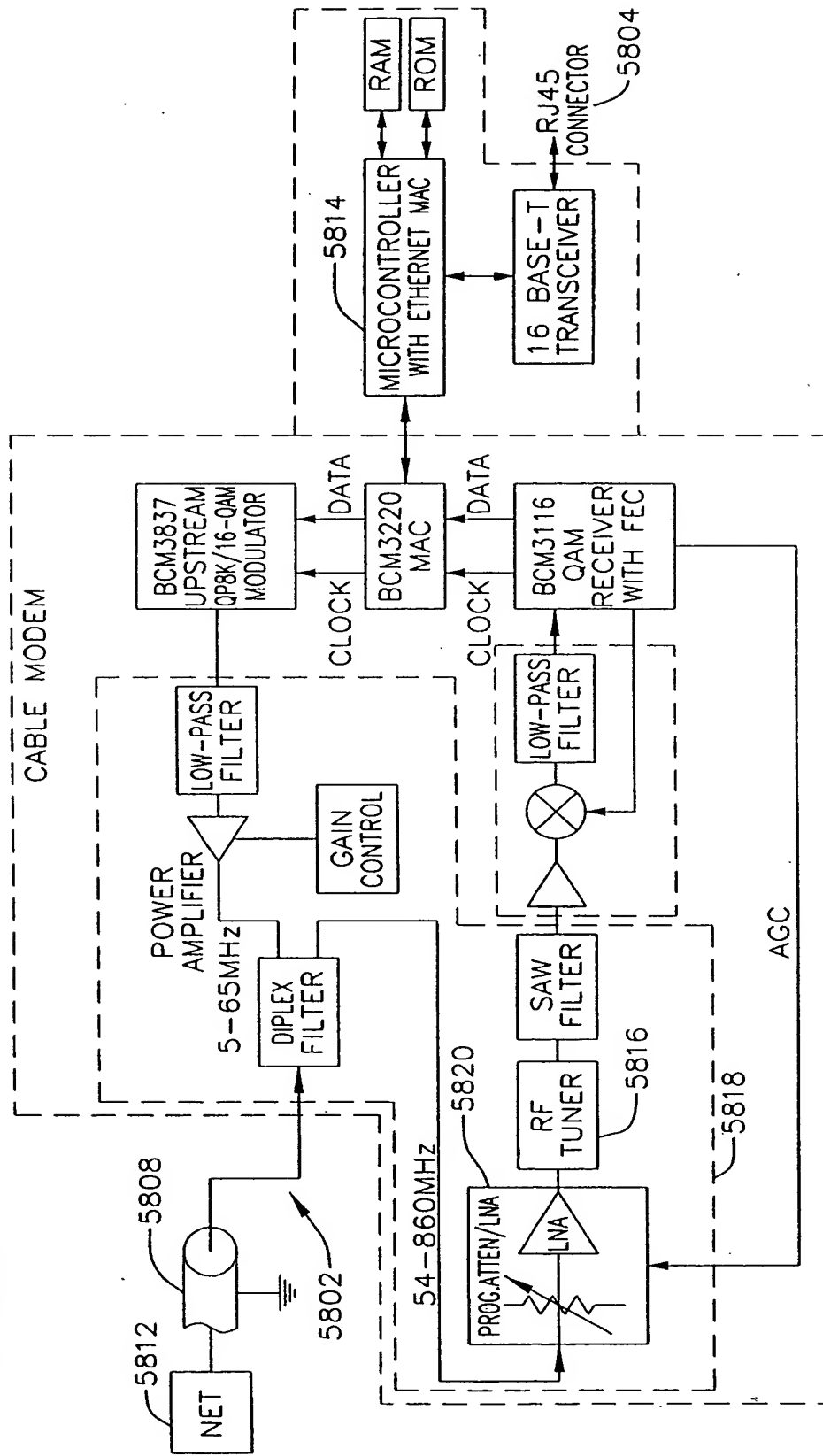
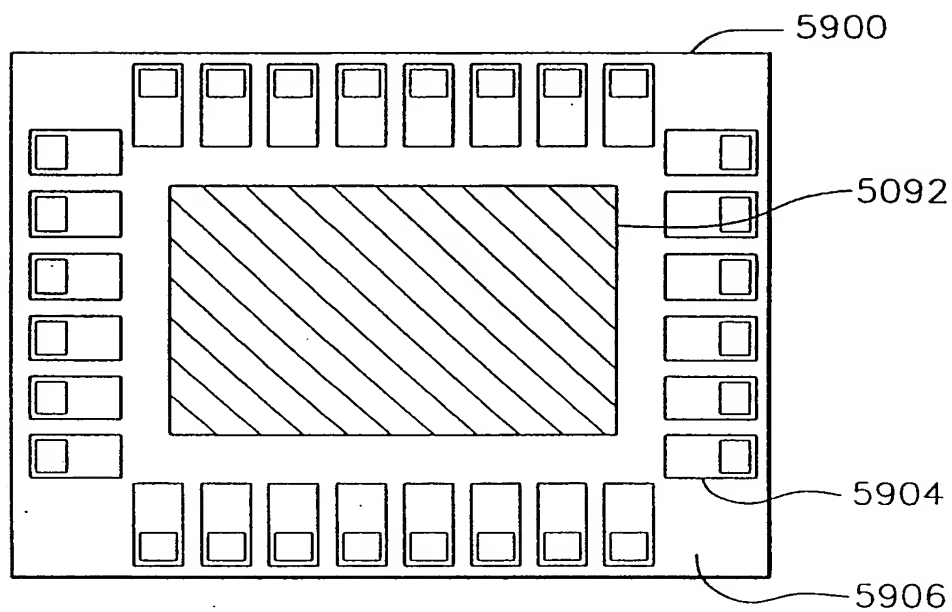


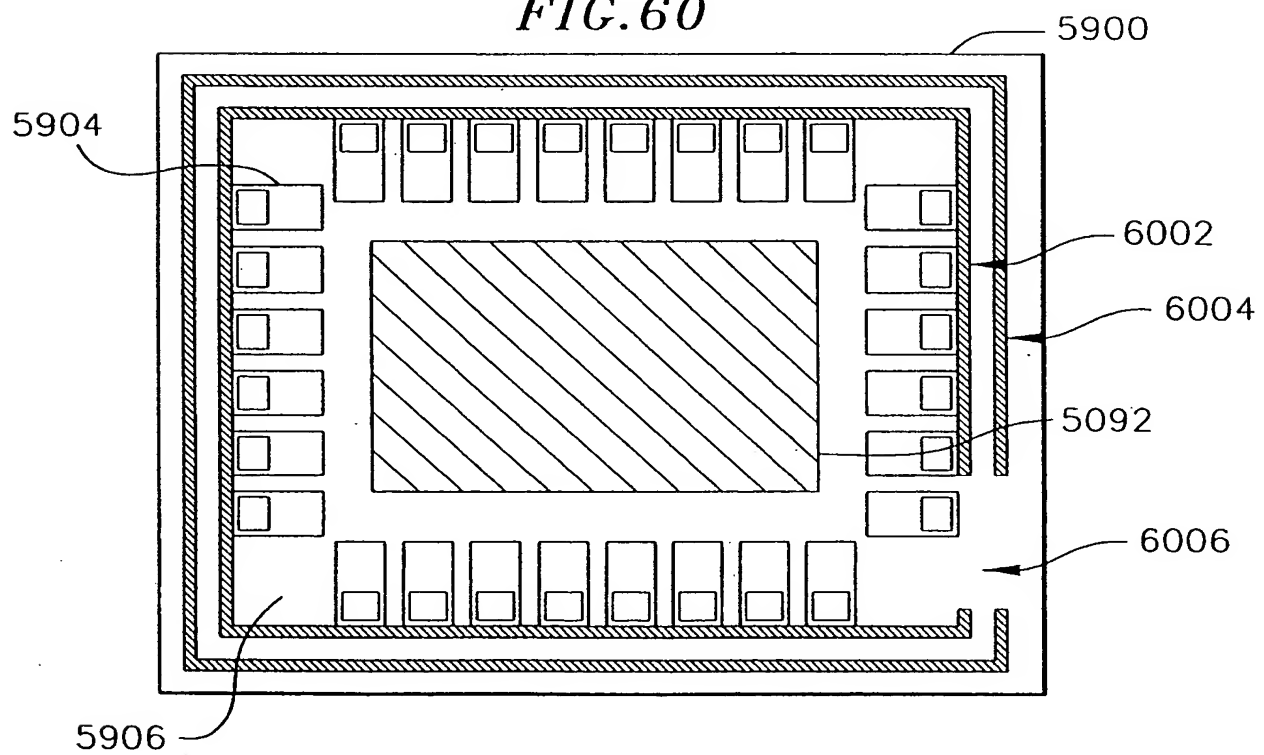
FIG. 58



*FIG. 59*



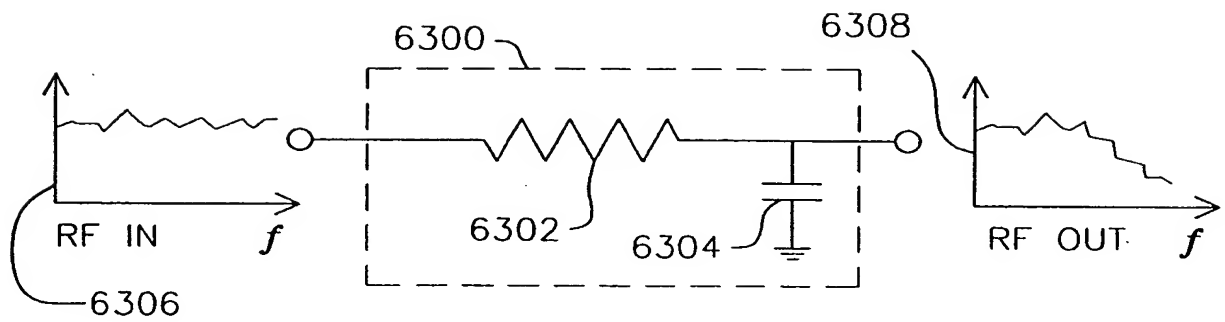
*FIG. 60*



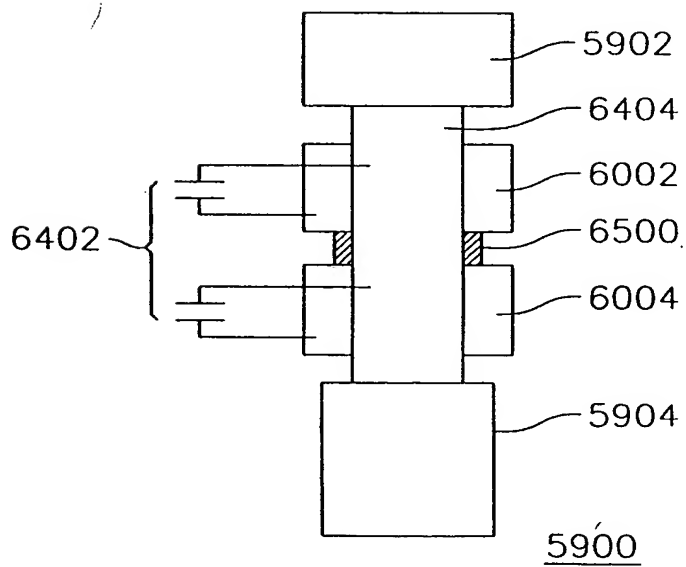
4)



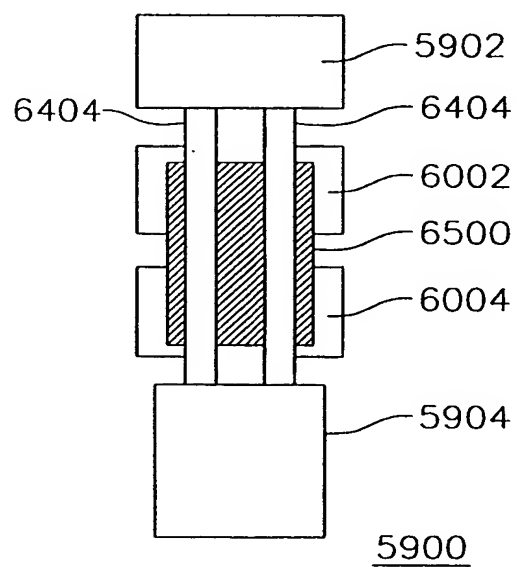
*FIG. 63*



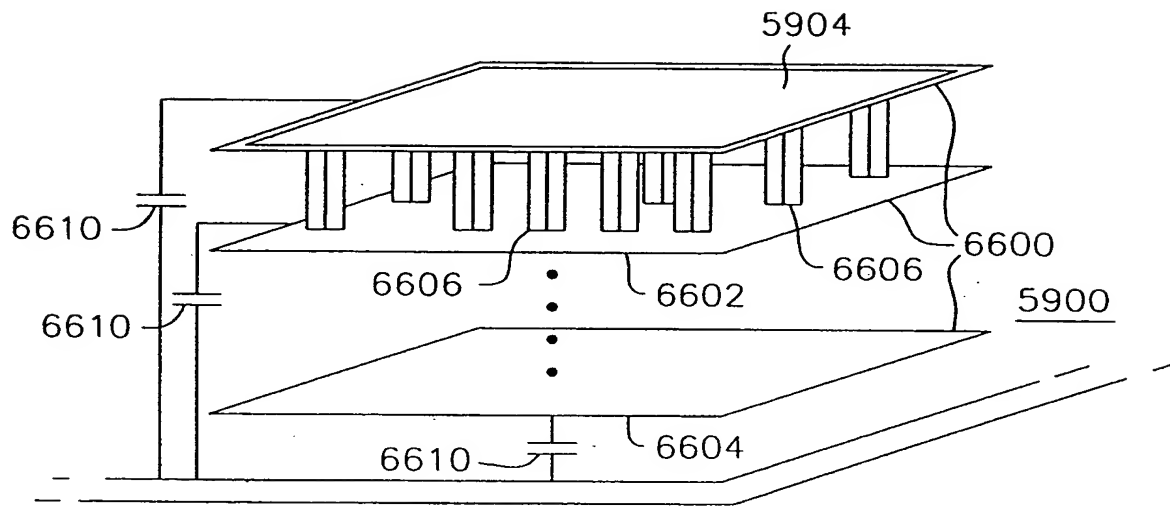
*FIG. 64*



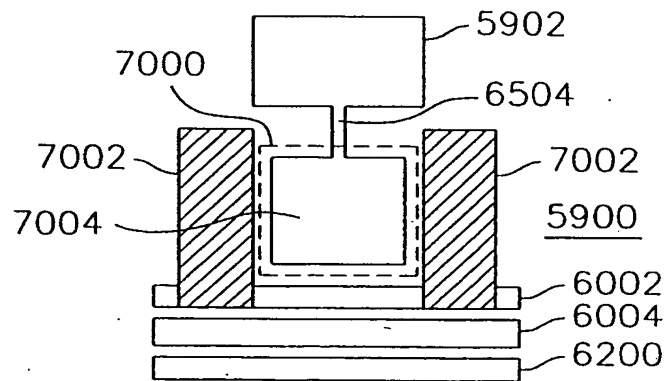
*FIG. 65*



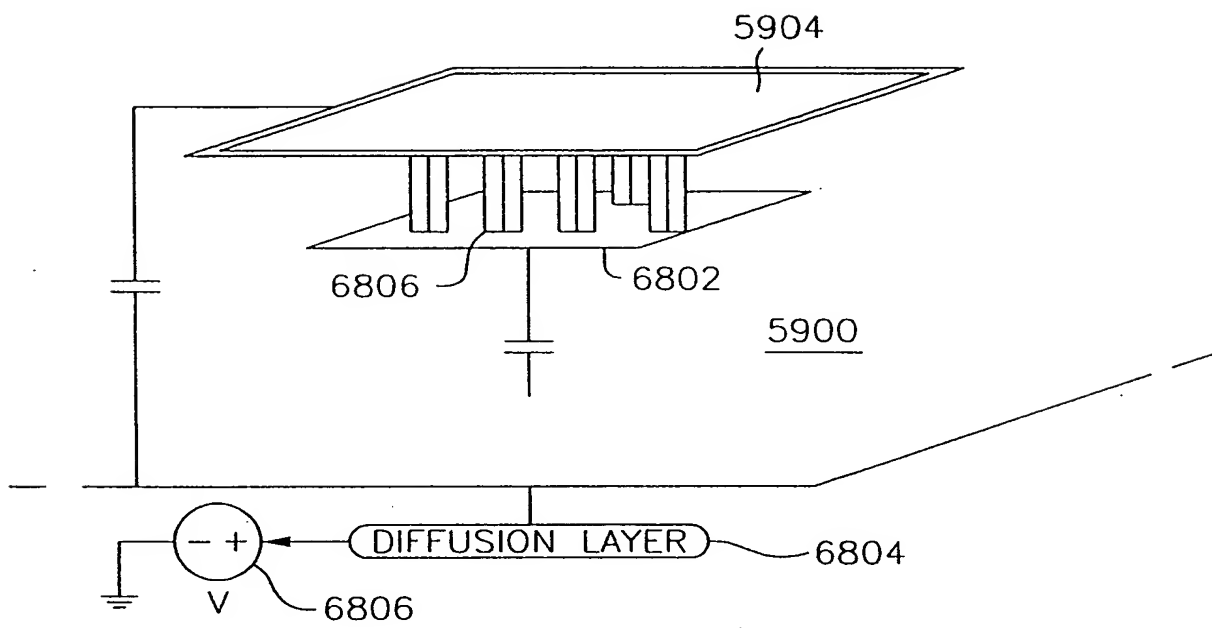
**FIG. 66**



**FIG. 67**



*FIG. 68*



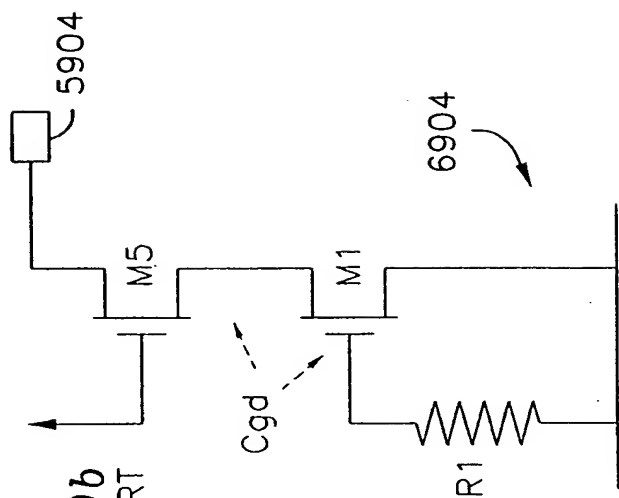


FIG. 69a  
PRIOR ART

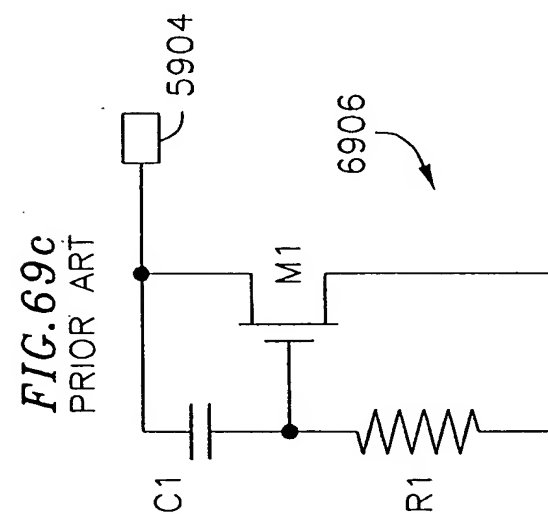
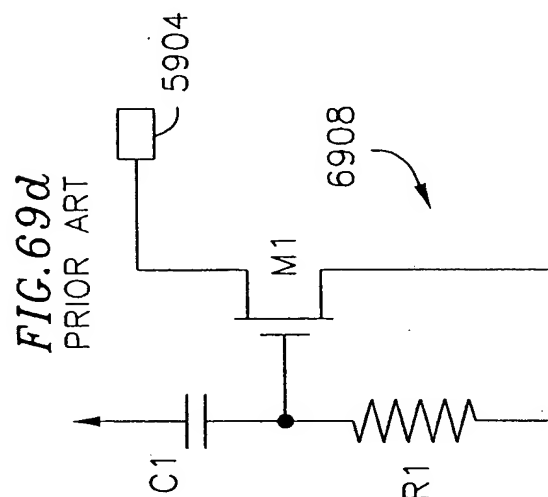
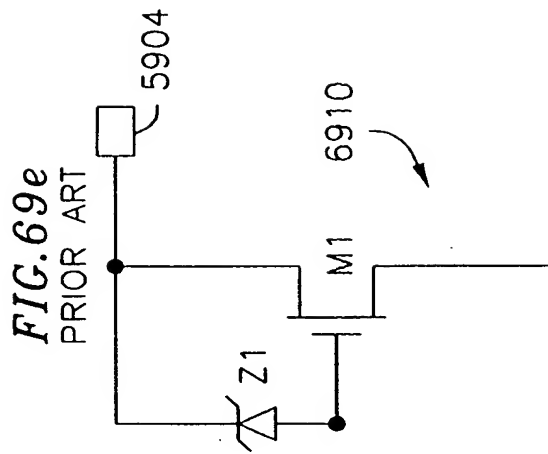
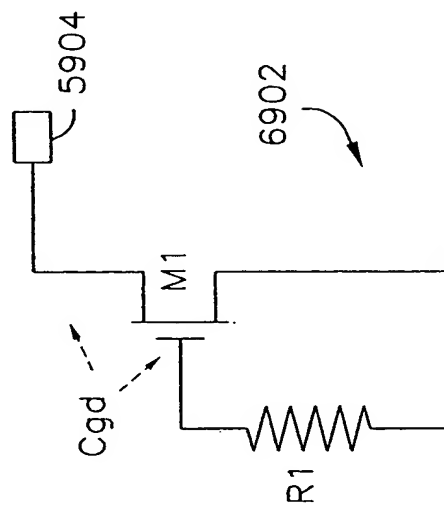
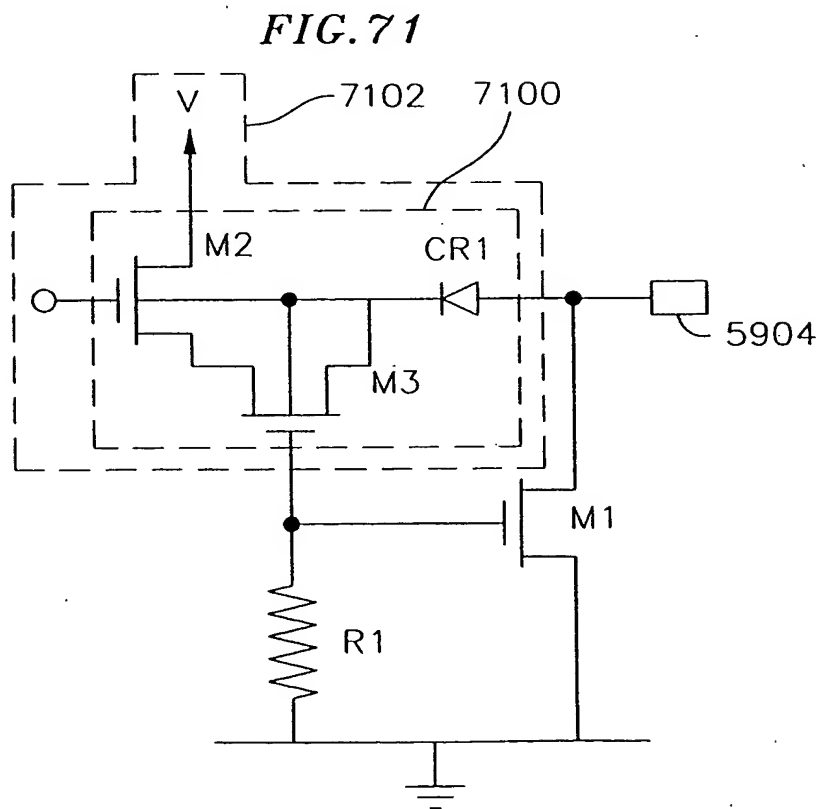
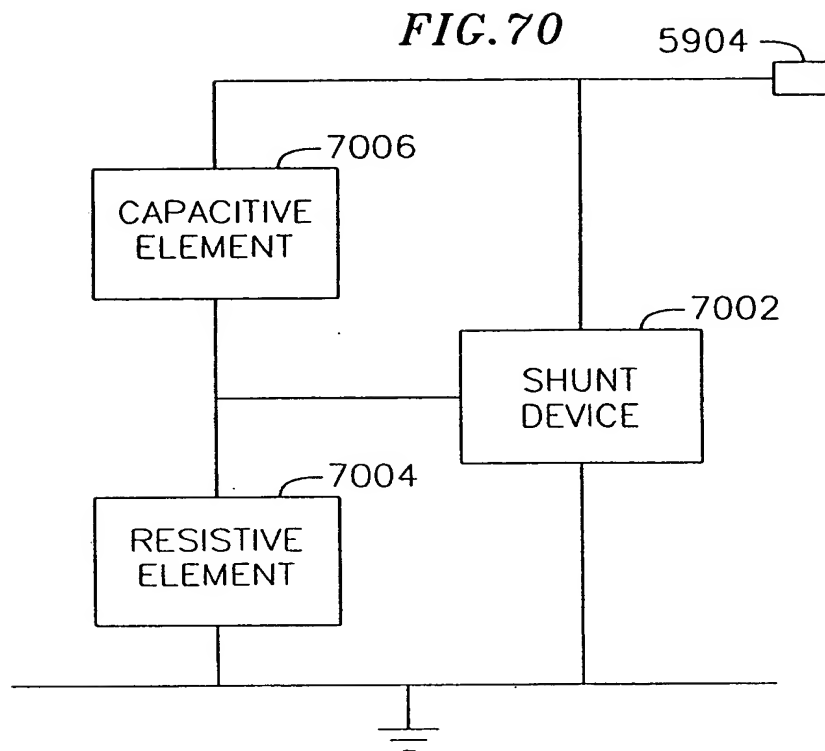
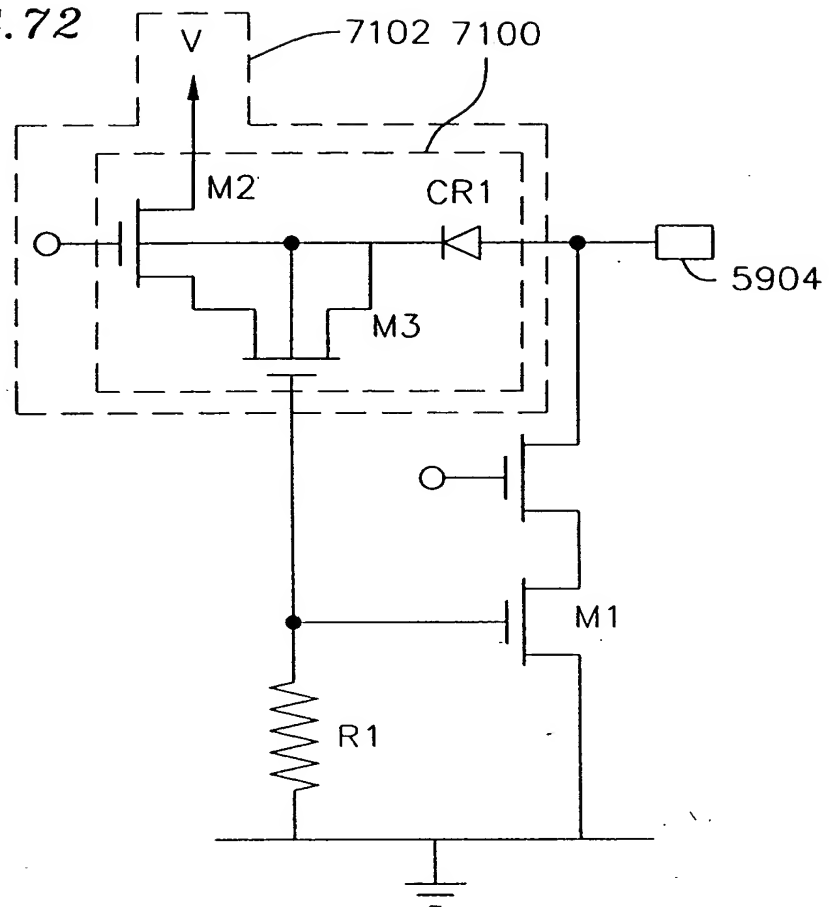


FIG. 69e  
PRIOR ART



**FIG. 72**



**FIG. 73**

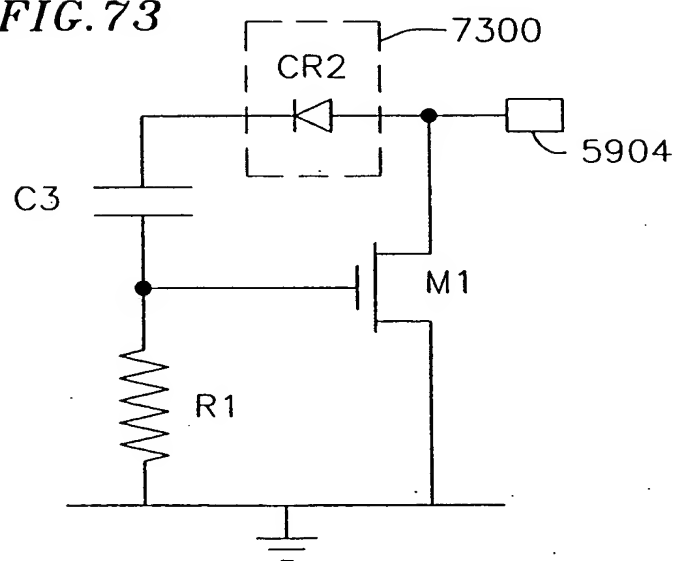


FIG. 74

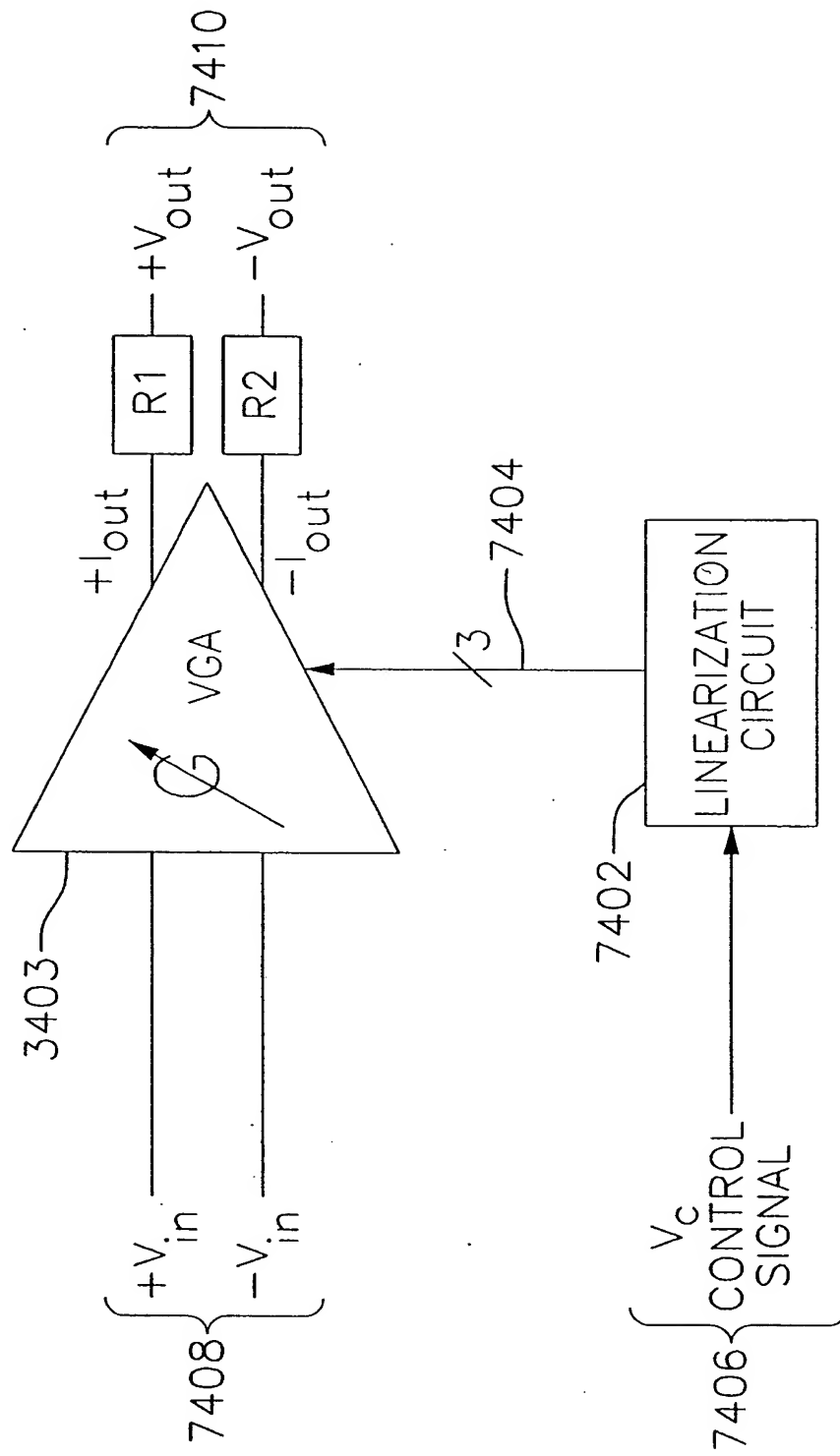
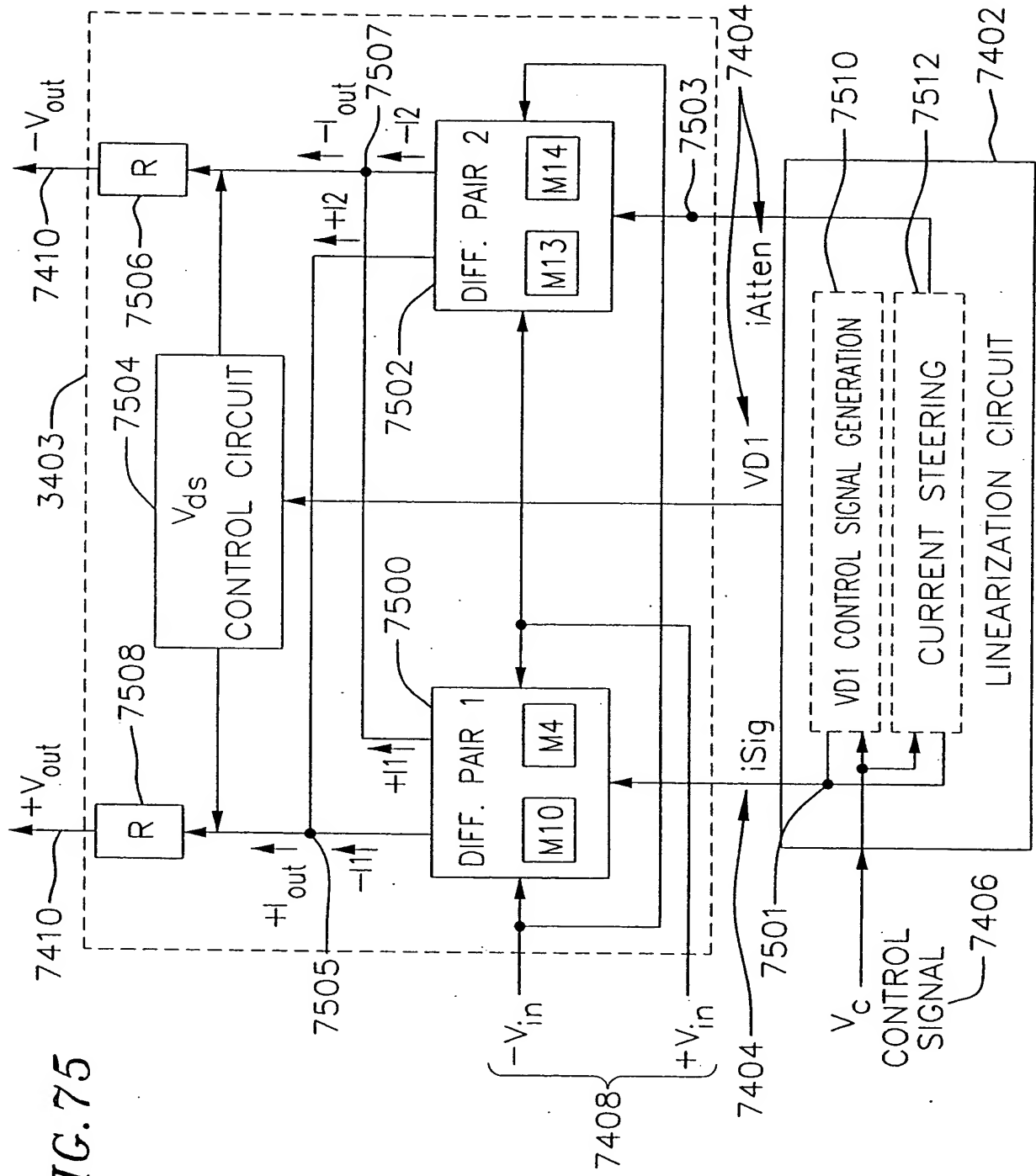
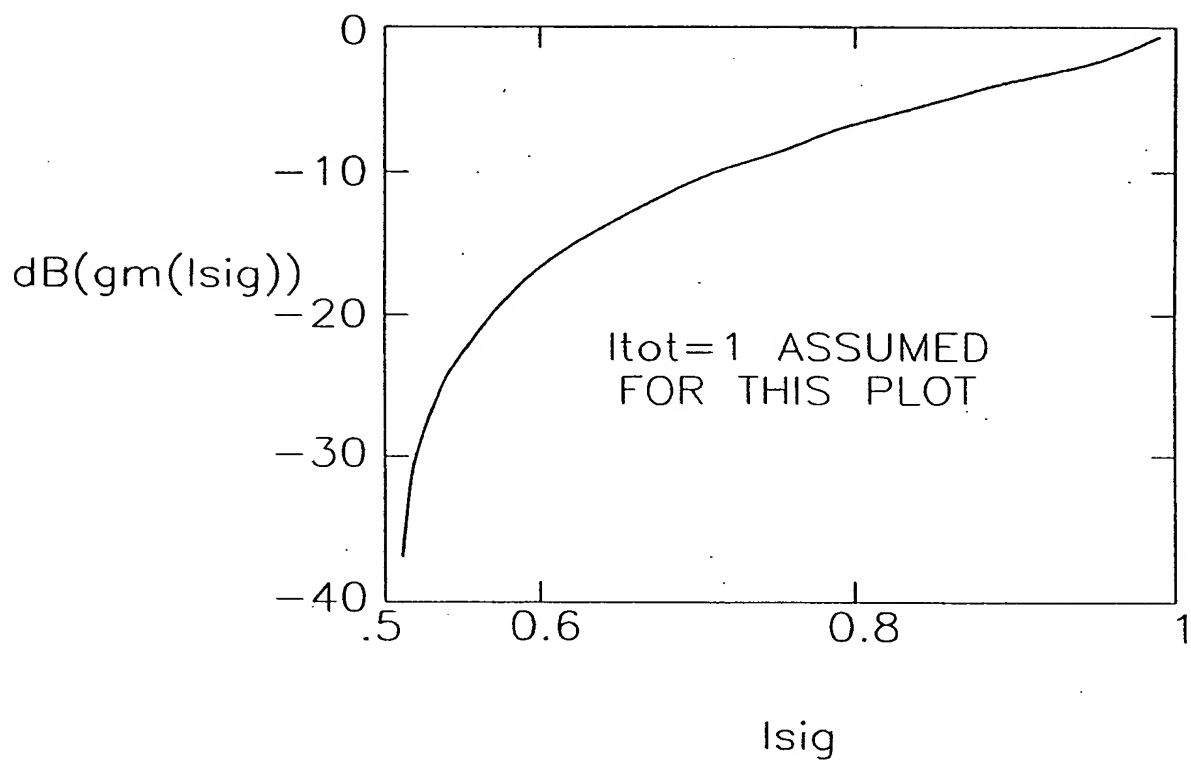


FIG. 75



**FIG. 76**



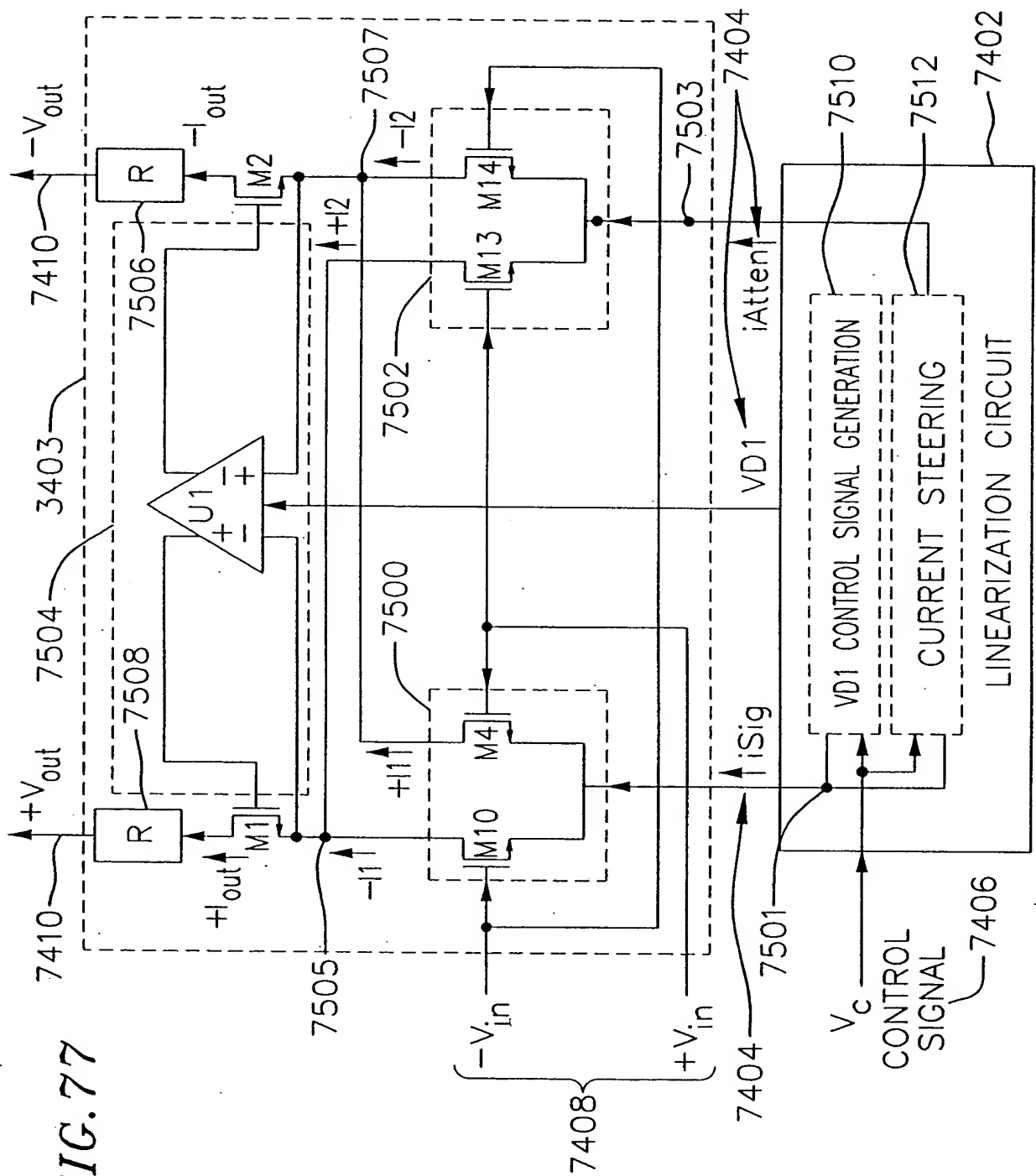
[illegible]

FIG. 78a

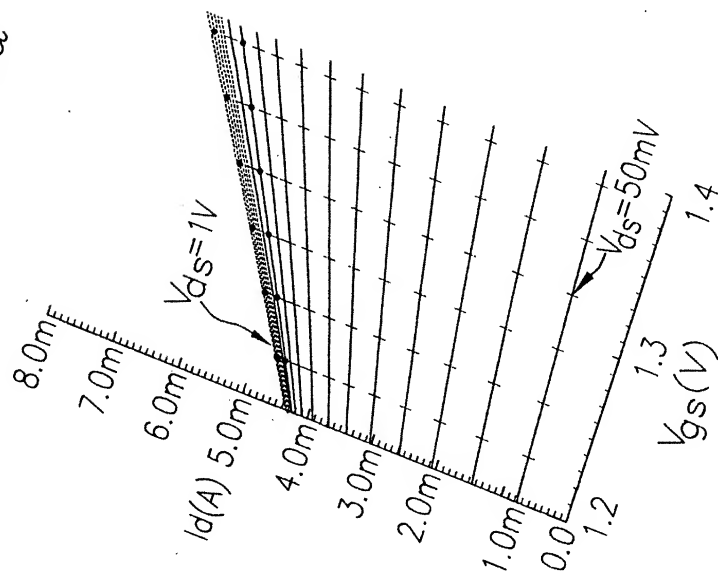
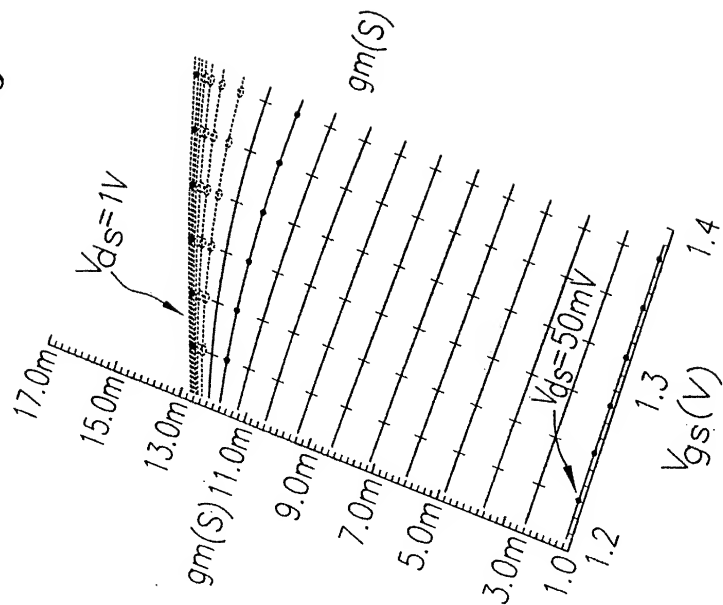


FIG. 78b



100

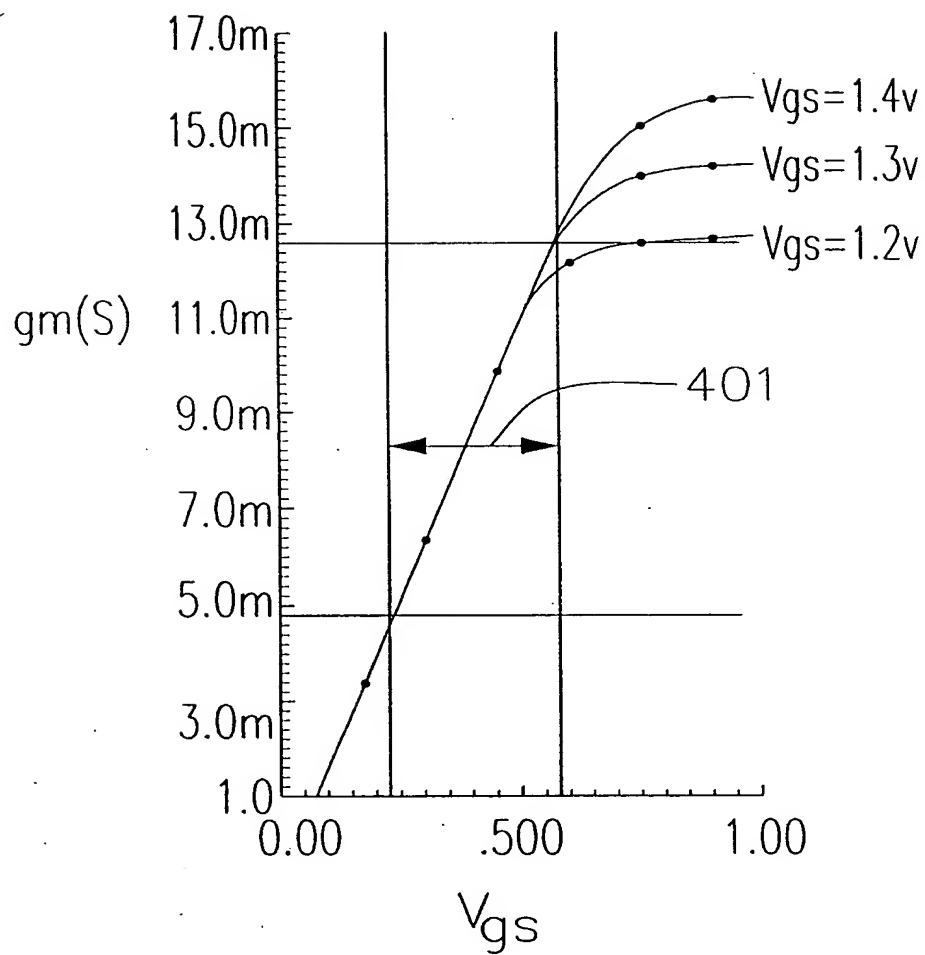


FIG. 79

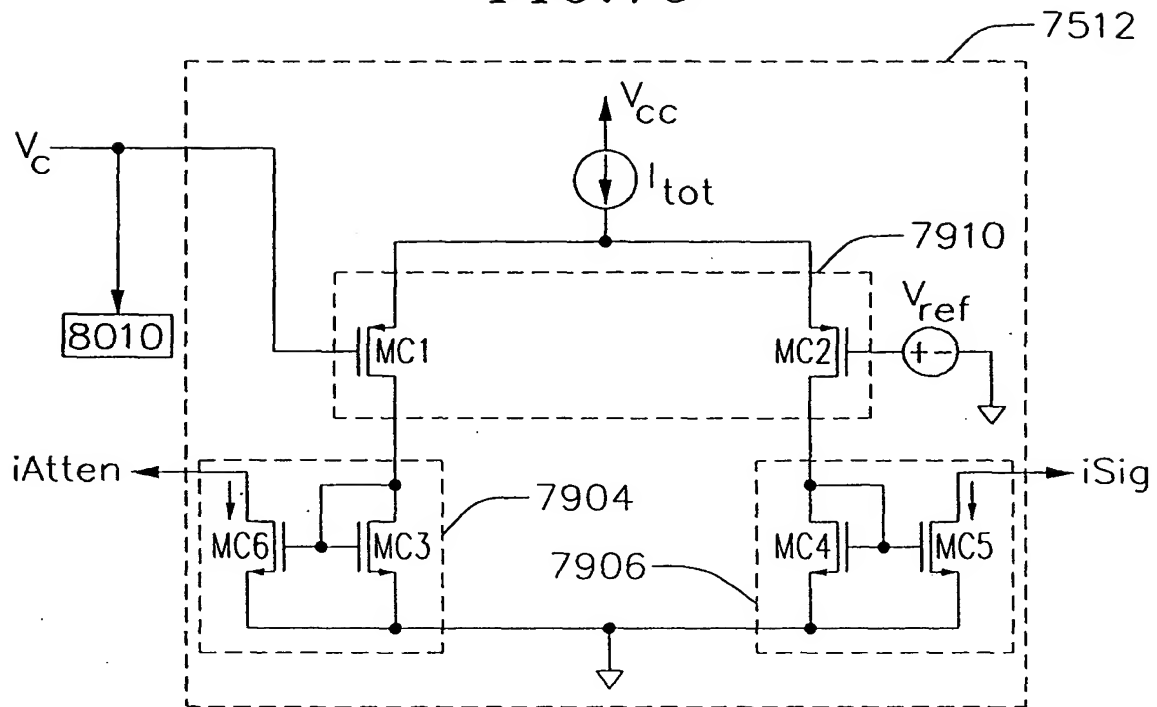


FIG. 80

